Ferroelectric ceramic capacitors: There is more than meets the eye

Presented at:

Tel Aviv 13 November 2019

VICOR

High-Performance Power Conversion Seminar & Workshops

Resources

This lecture is recorded and be available at the YouTube channel:
https://www.youtube.com/user/sambenyaakov/videos

LinkedIn Group ” **Where analog and power electronics meet knowledge** “
https://www.linkedin.com/groups/13606756

Papers and university lectures
http://www.ee.bgu.ac.il/~pel/

sby@bgu.ac.il

Thanks to Mr. Evgeny Rozanov assisting in the preparation of this presentation

Background

Ceramic capacitors are one of the most popular electronic devices. They are used for filtering, decoupling and bypass. And yet, not all the features of these devices are understood or even known.

Objective

To present unfamiliar characteristics of ceramic capacitors (especially ferroelectric type) relevant to power electronics.

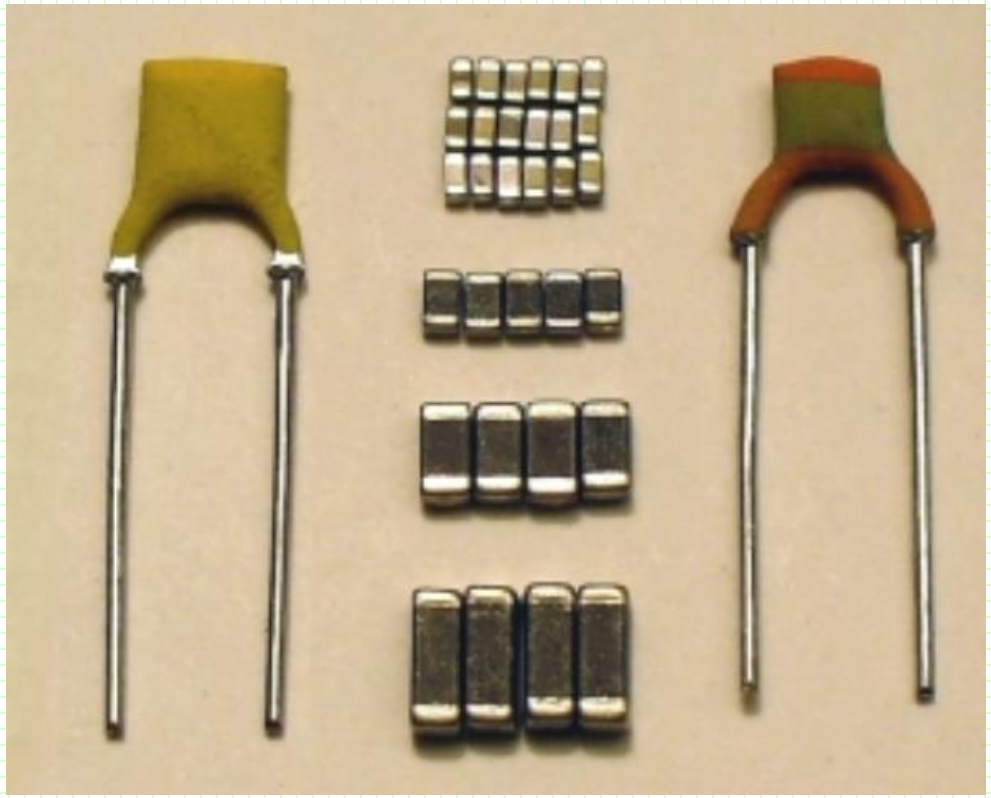
- For ceramic capacitor types and classification see https://en.wikipedia.org/wiki/Ceramic_capacitor

Outline

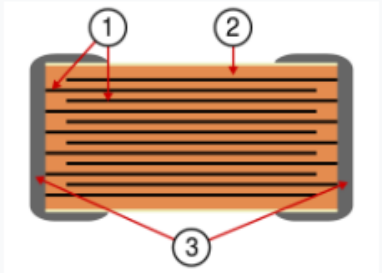
1. General specifications of commercial ceramic capacitors
2. ESR as a function of bias voltage
3. Piezoelectricity
4. Nonlinear capacitor modeling

General specifications of commercial ceramic capacitors

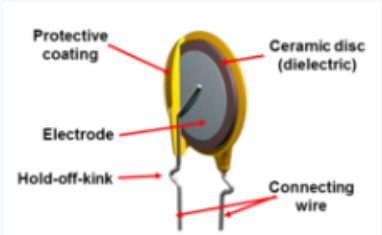
Structure of ceramic capacitors



Basic structure of ceramic capacitors



Construction of a multilayer ceramic chip capacitor (MLCC), 1 = Metallic electrodes, 2 = Dielectric ceramic, 3 = Connecting terminals

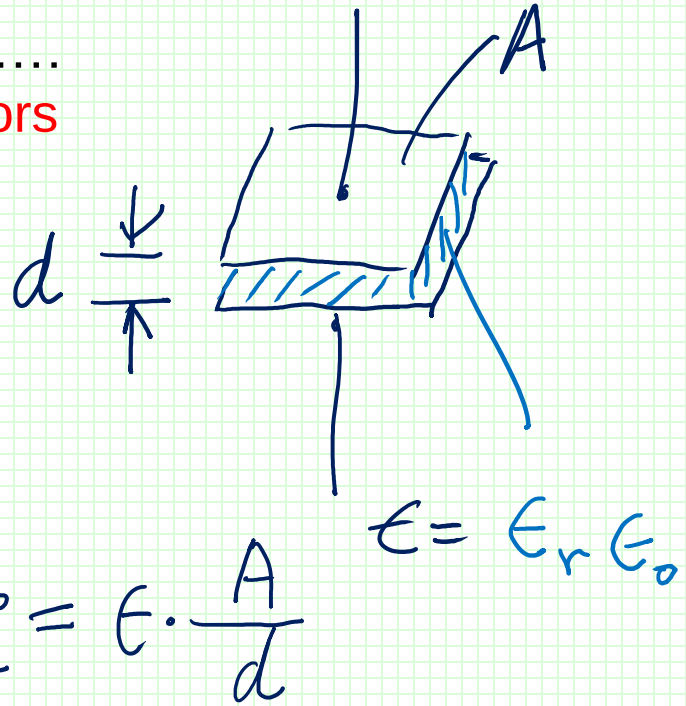


Construction of a ceramic disc capacitor

Wikipedia

Commercial Ceramic capacitors

- Practical ceramic capacitors are build around paraelectric (Class I) and ferroelectric (Class II,III) dielectric materials
- Predominant Class I material is C0G (NPO) – low dielectric constant
- Class II, III includes different dielectric materials e.g. X7R, Y5V ……
  High dielectric constant, Class III the highest, small capacitors
- Single, or multilayer (MLCC)



Ferroelectric – dependence on electric field
Similar to ferromagnetic – dependence on magnetic field
Has nothing to do with ferro (iron)!

Different definitions of application classes for ceramic capacitors

Definition regarding to IEC/EN 60384-1 and IEC/EN 60384-8/9/21/22	Definition regarding to EIA RS-198
Class 1 ceramic capacitors offer high stability and low losses for resonant circuit applications.	**Class I** (or written class 1) ceramic capacitors offer high stability and low losses for resonant circuit application
Class 2 ceramic capacitors offer high volumetric efficiency for smoothing, by-pass, coupling and decoupling applications	**Class II** (or written class 2) ceramic capacitors offer high volumetric efficiency with change of capacitance lower than −15% to +15% and a temperature range greater than −55 °C to +125 °C, for smoothing, by-pass, coupling and decoupling applications
Class 3 ceramic capacitors are barrier layer capacitors which are not standardized anymore	**Class III** (or written class 3) ceramic capacitors offer higher volumetric efficiency than EIA class II and typical change of capacitance by −22% to +56% over a lower temperature range of 10 °C to 55 °C. They can be substituted with EIA class 2-Y5U/Y5V or Z5U/Z5V capacitors
-	**Class IV** (or written class 4) ceramic capacitors are barrier layer capacitors which are not standardized anymore

Paraelectric - COG (NPO)
Small ε_r , smaller ESR

Ferroelectric
Large ε_r, larger ESR

Feroelectricity - Electric polarization

Let a volume dV be isolated inside the dielectric. Due to polarization the positive bound charge $\mathrm{d}q_b^+$ will be displaced a distance $\mathbf{d}$ relative to the negative bound charge $\mathrm{d}q_b^-$, giving rise to a dipole moment $\mathrm{d}\mathbf{p} = \mathrm{d}q_b\mathbf{d}$. Substitution of this expression in (1) yields

$$\mathbf{P} = \frac{\mathrm{d}q_b}{\mathrm{d}V}\mathbf{d}$$

Since the charge $\mathrm{d}q_b$ bounded in the volume dV is equal to $\rho_b \mathrm{d}V$ the equation for **P** becomes:[3]

$$\mathbf{P} = \rho_b\mathbf{d} \qquad (2)$$

where ρ_b is the density of the bound charge in the volume under consideration.

Polarization: a measure of electric dipole moment, ability to bound charge

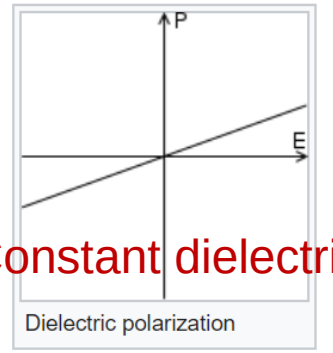
In a homogeneous, linear and isotropic dielectric medium, the **polarization** is aligned with and proportional to the electric field **E**:[7]

$$\mathbf{P} = \chi\varepsilon_0\mathbf{E},$$

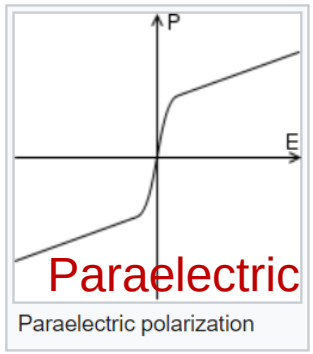
where ε_0 is the electric constant, and χ is the electric susceptibility of the medium. Note that in this case χ simplifies to a scalar, although more generally it is a tensor. This is a particular case due to the *isotropy* of the dielectric.

In electricity (electromagnetism), the **electric susceptibility** (χ_e; Latin: *susceptibilis* "receptive") is a dimensionless proportionality constant that indicates the degree of polarization of a dielectric material in response to an applied electric field. The greater the electric susceptibility, the greater the ability of a material to polarize in response to the field, and thereby reduce the total electric field inside the material (and store energy). It is in this way that the electric susceptibility influences the electric permittivity of the material and thus influences many other phenomena in that medium, from the capacitance of capacitors to the speed of light.[1][2]

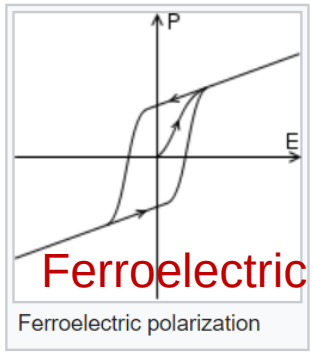
Electric polarization of dielectric materials
Paraelectricity, ferroelectricity



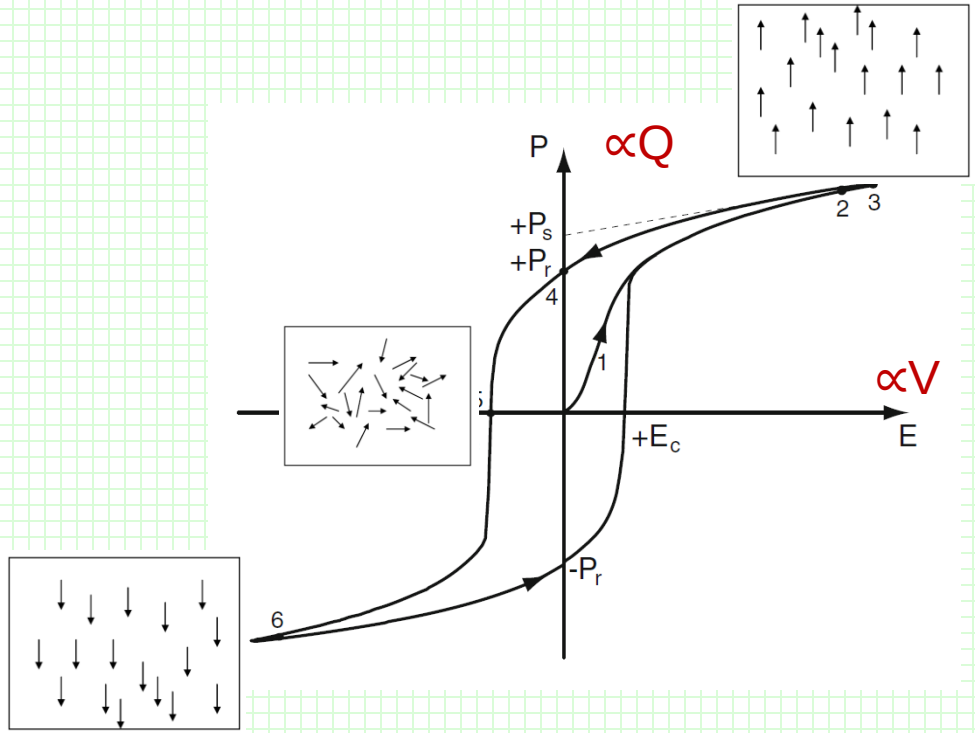
Constant dielectric



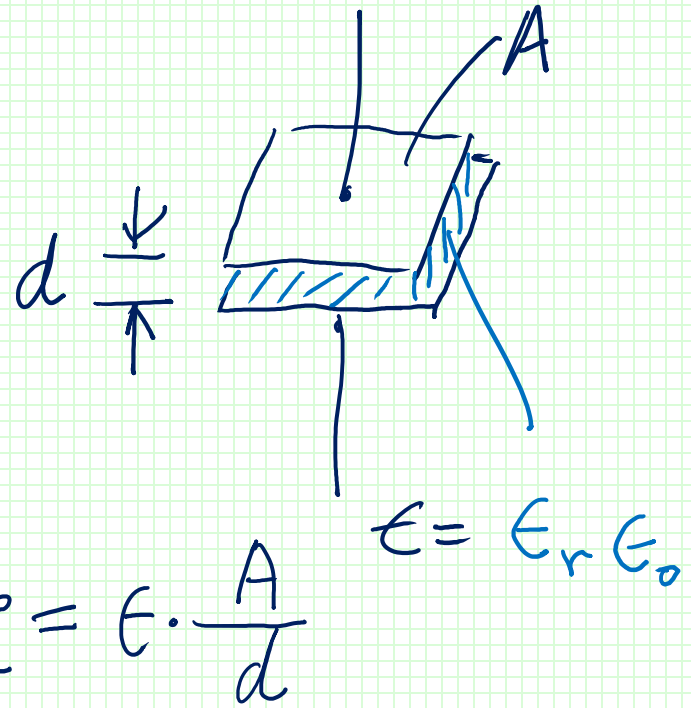
Paraelectric



Ferroelectric



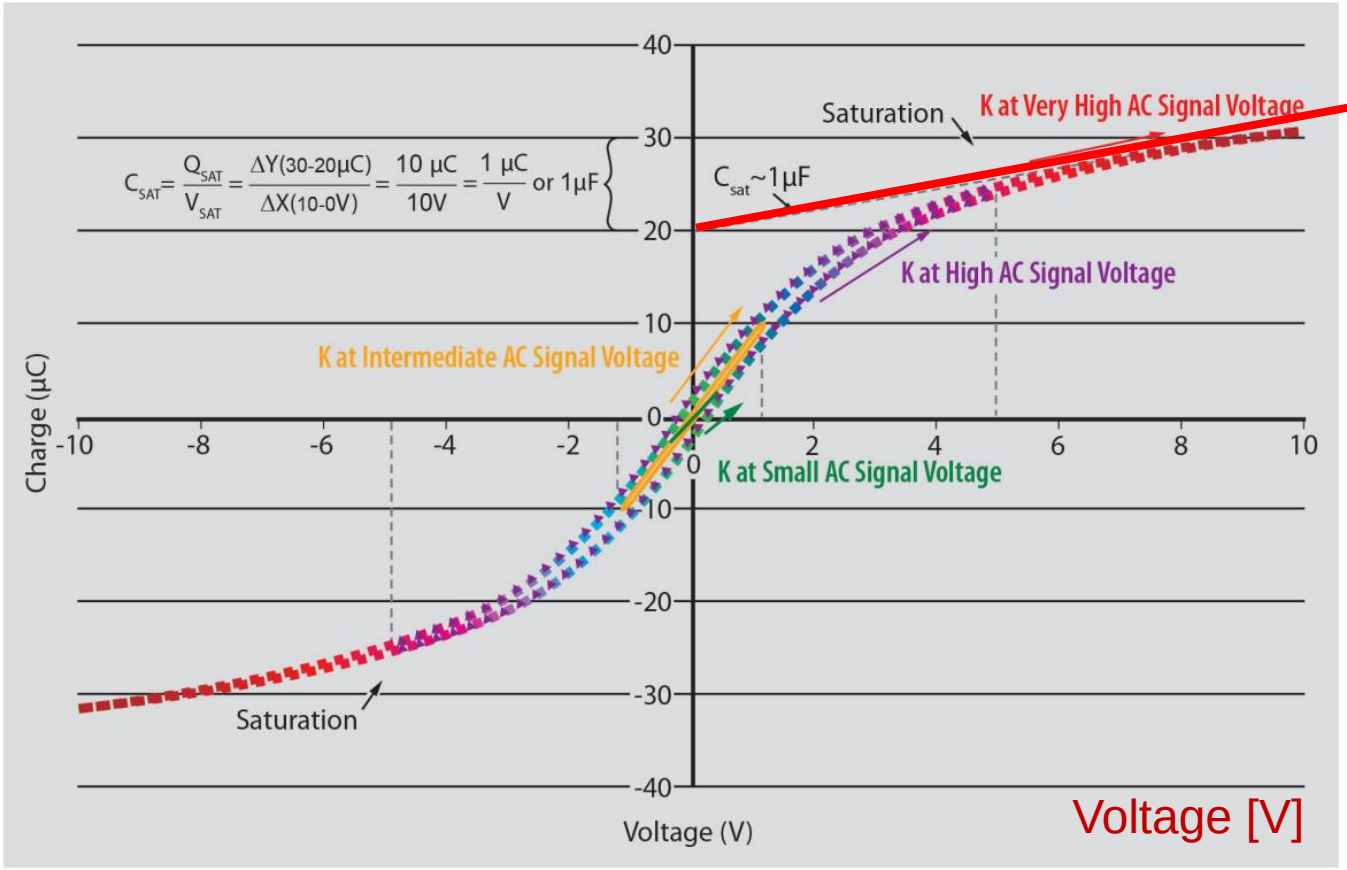
Ferroelectric material



ε_r of ferroelectric material is very large up to 7000
Small capacitors

Ferroelectric hysteresis and capacitance

Charge [Q]



$$C_d = \frac{dQ}{dV}$$

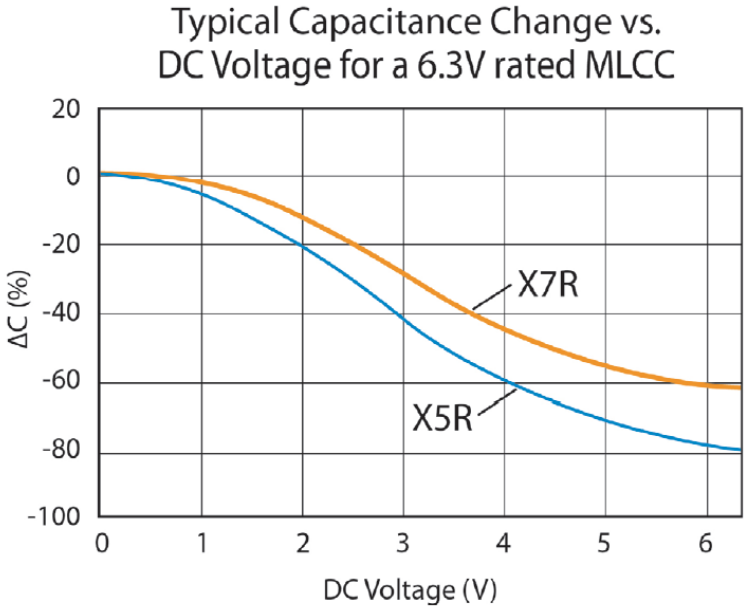
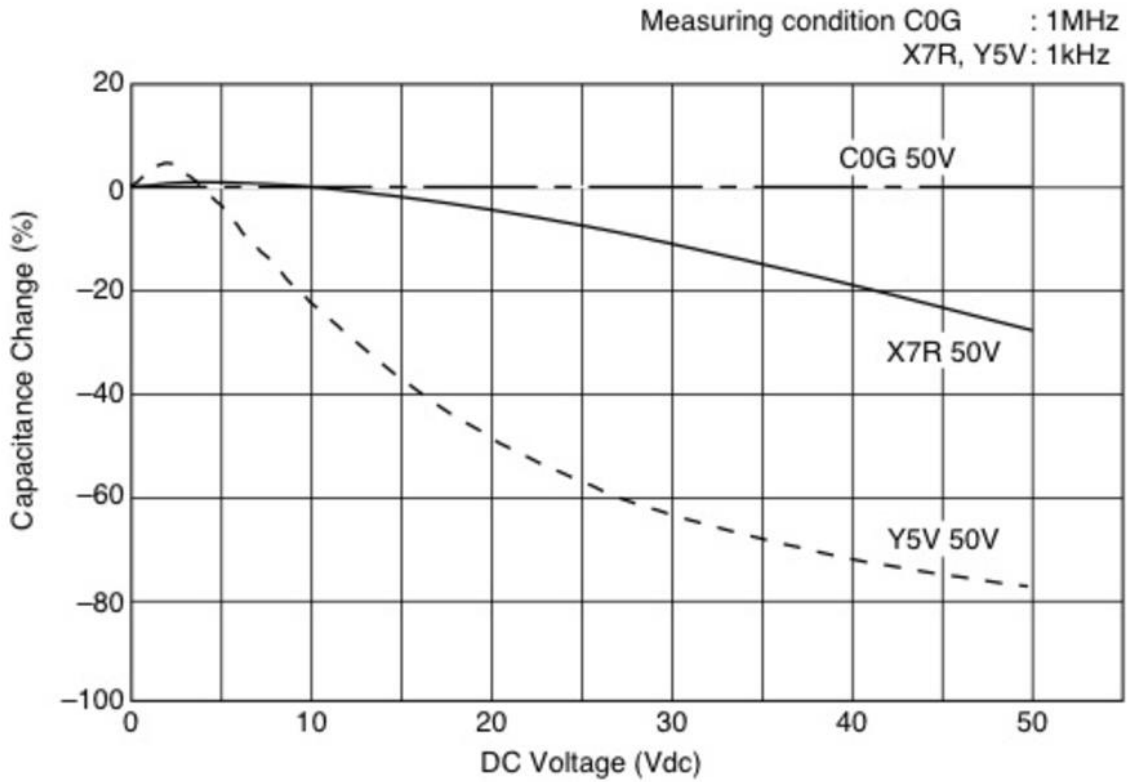


Figure 11. Hysteresis curve for a 10μF ferroelectric dielectric as a function of AC test signal voltage.

■ Capacitance - DC Voltage Characteristics



Commercial paraelectric ceramic capacitors (C0G) are limited to about 0.1μF

Temperature dependence

Standard	Characteristics	Basic temperature	Temperature range	Capacitance tolerance
JIS	B	20°C	-25～+85°C	±15%
EIA	X5R	25°C	-55～+85°C	±15%
	X5S			±22%
	X5T			+22%, -33%
	X6S		-55～+105°C	±22%
	X6T			+22%, -33%
JIS	R	20°C	-55～+125°C	±15%
EIA	X7R	25°C	-55～+125°C	±15%
	X7S			±22%
	X7T			+22%, -33%
	X7U			+22%, -56%
	X8R		-55～+150°C	±15%
JIS	F	20°C	-25～+85°C	+30%, -80%
EIA	Y5V	25°C	-30～+85°C	+22%, -82%
	Z5U		+10～+85°C	+22%, -56%
	Z5V			+22%, -82%

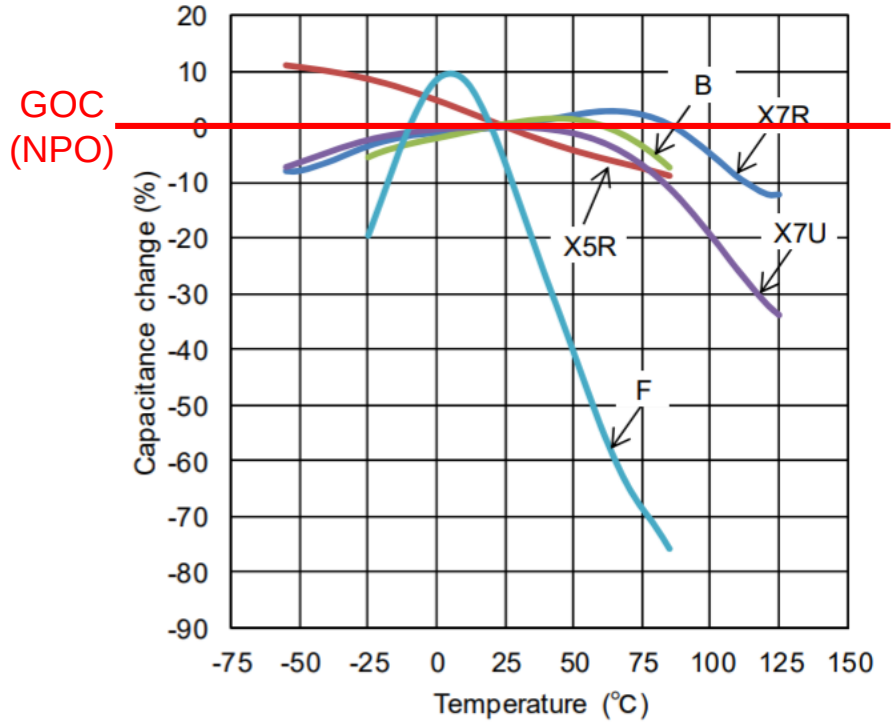
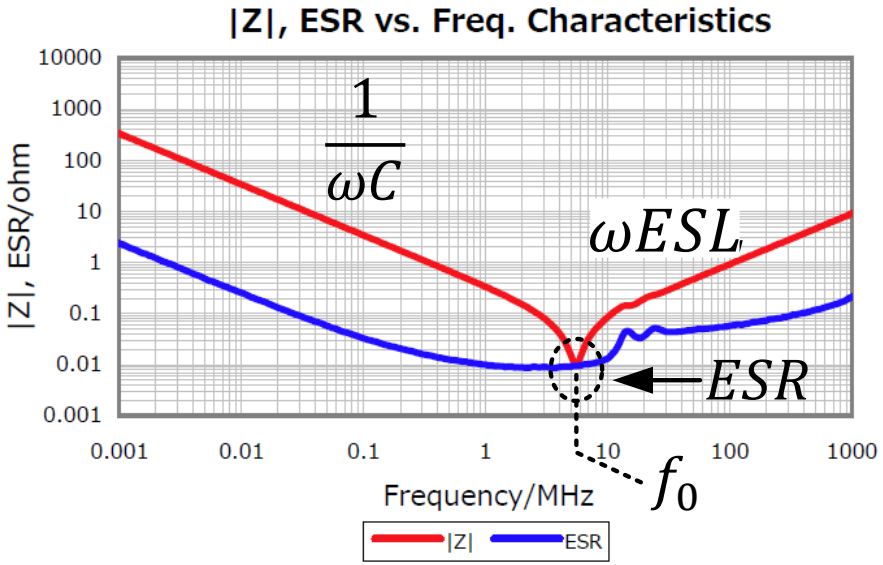
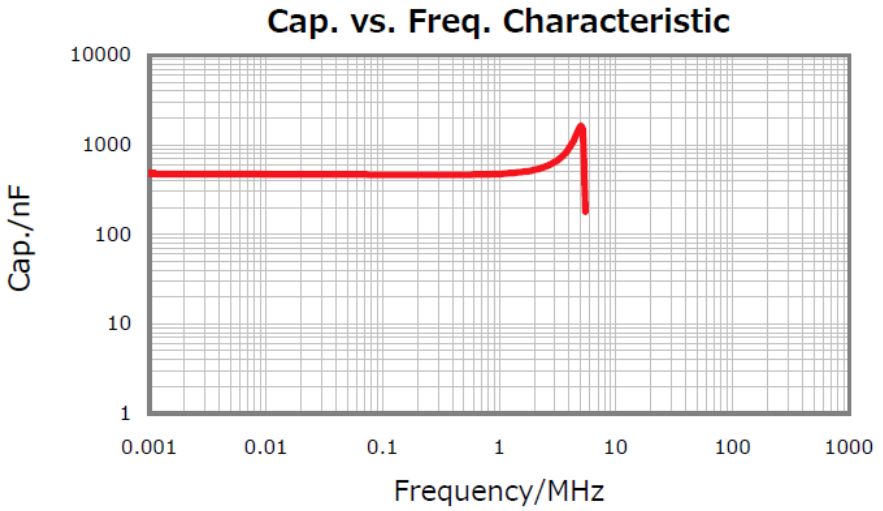


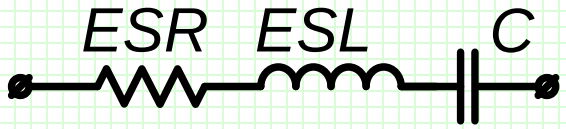
Figure 2. Major Temperature Characteristics of High-dielectric constant type MLCC

EIA - Electronic Industries Alliance JIS - Japanese Industrial Standards

Typical ceramic capacitor data sheet parameters

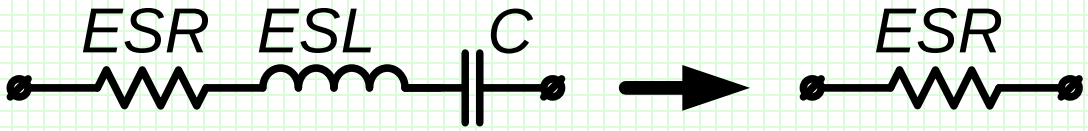






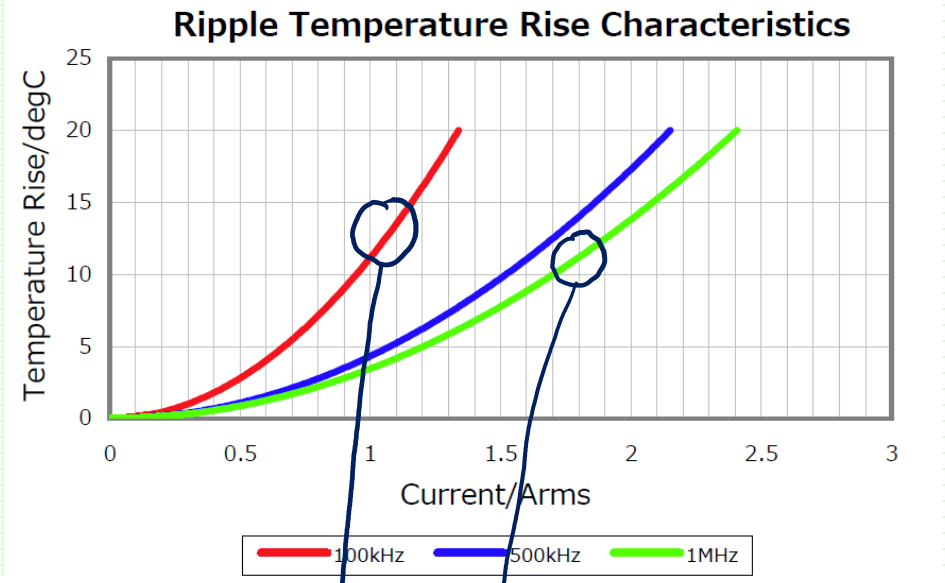
$$\omega_0 = \frac{1}{\sqrt{LC}} \qquad f_0 = \frac{1}{2\pi\sqrt{LC}}$$

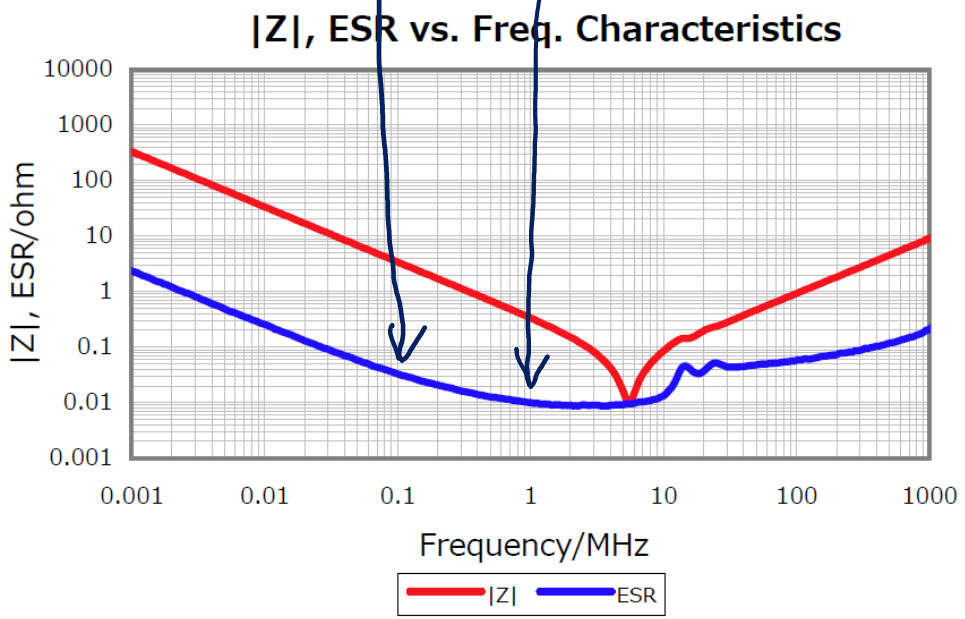
At resonance:



$$f < f_0 : \; Z = \frac{1}{\omega C}$$

$$f > f_0 : \; Z = \omega ESL$$

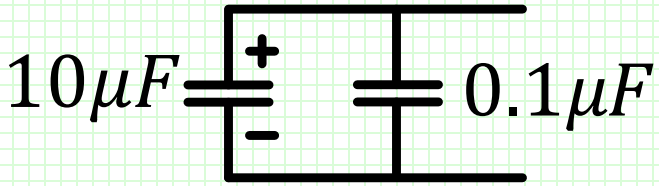


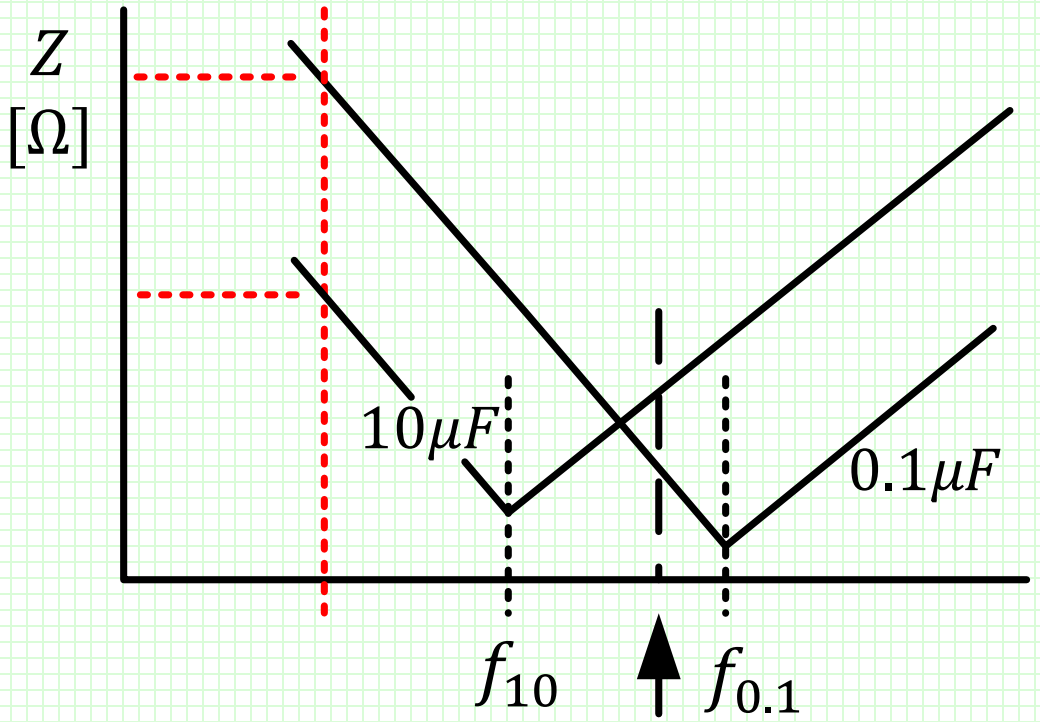


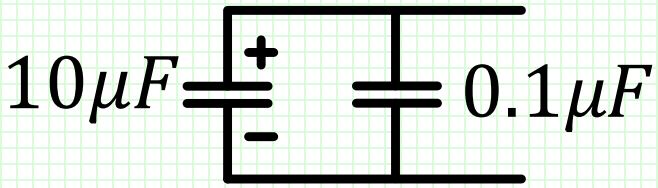
$$P = i_{rms}^2 \cdot ESR$$

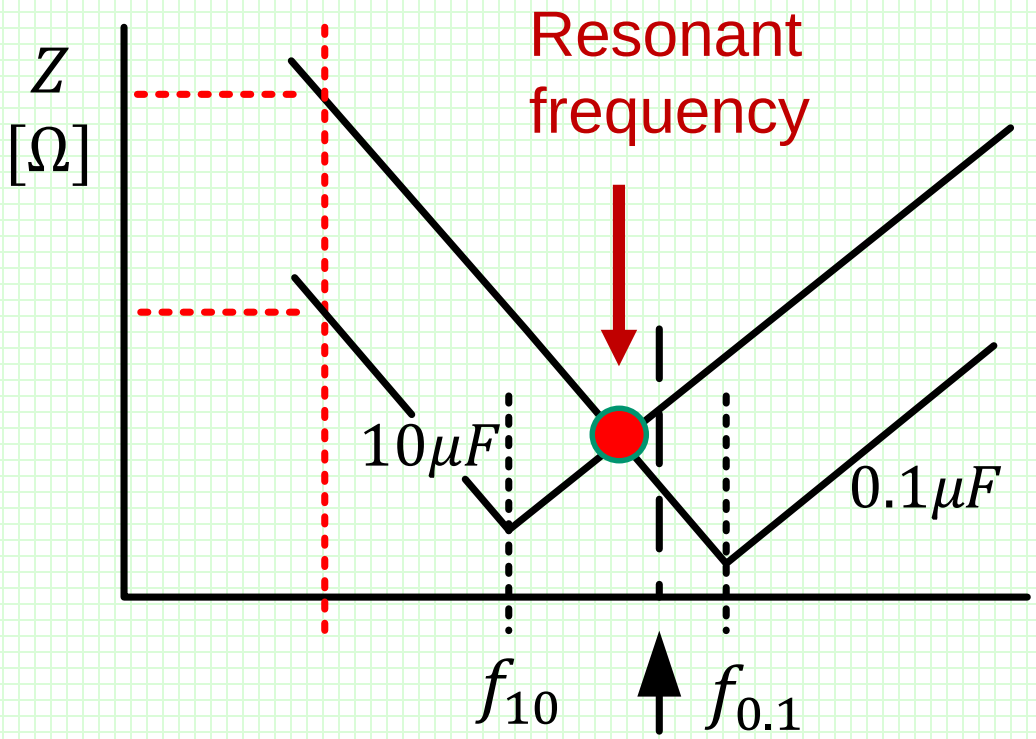
$$\Delta T = P \cdot R_{termal}$$

Why 0.1uF in parallel to a larger capacitor?







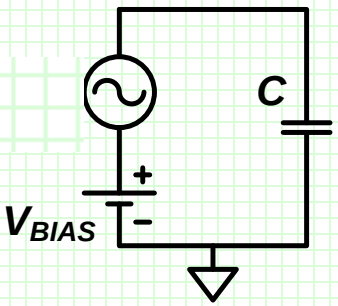


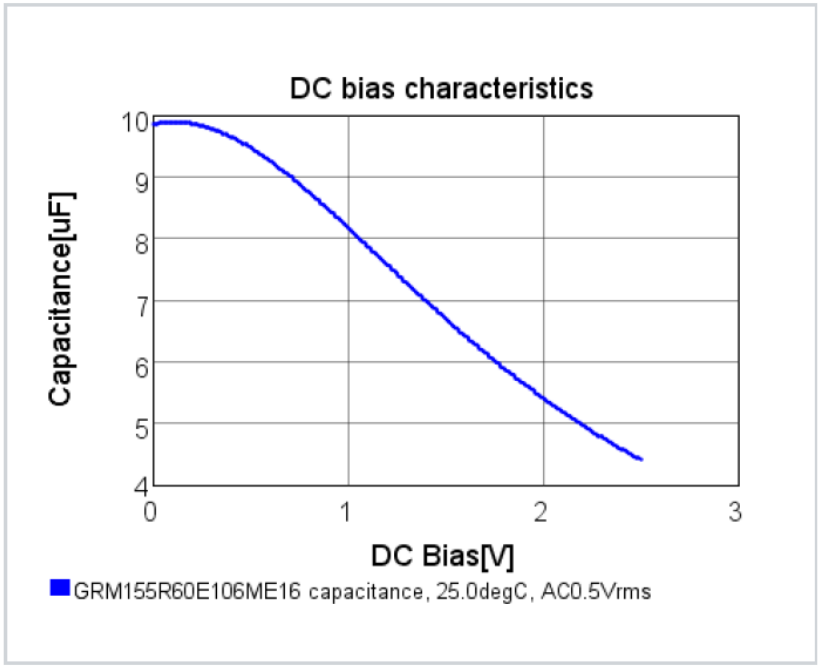
$$\omega L = \frac{1}{\omega C}$$

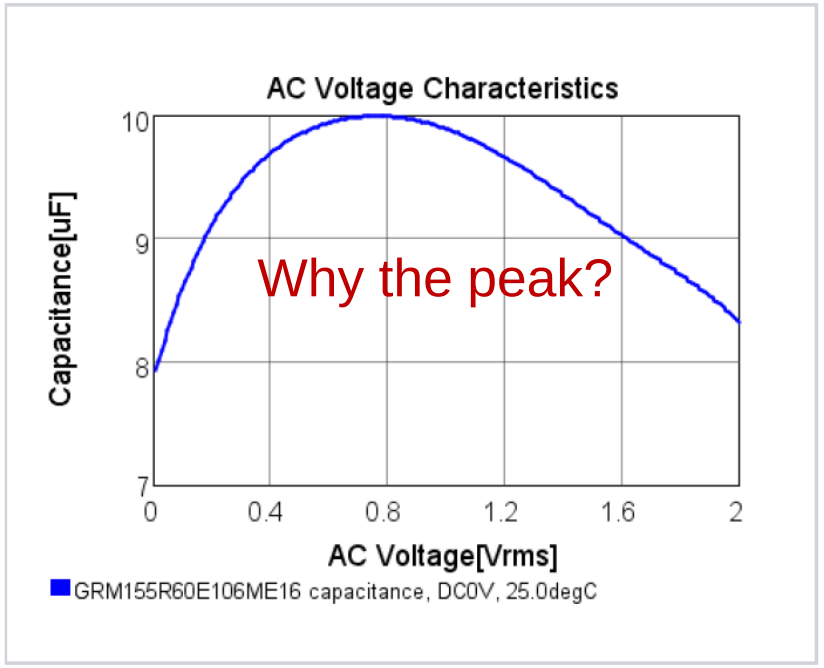
$$\omega = \frac{1}{\sqrt{LC}}$$

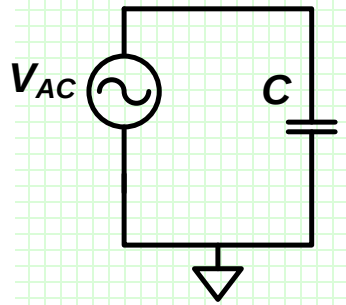
Capacitance definition (?)

$0.5V_{rms}$









1kHz

Local, Small signal, C_d Large signal C_{ac}

(No endorsement/affiliation implied)

The effect of size on C=f(V_{bias})

maxim integrated™

Maxim > Design Support > Technical Documents > Tutorials > General Engineering Topics > APP 5527

Keywords: cap, capacitor, capacitance, bypass, component variation, RC, X7R, X5R, ceramic, Y5V, passive

TUTORIAL 5527

Temperature and Voltage Variation of Ceramic Capacitors, or Why Your 4.7µF Capacitor Becomes a 0.33µF Capacitor

voltage behavior of several 16V, 1.0µF X7R caps versus their 4.7µF, 16V, X7R cousins.

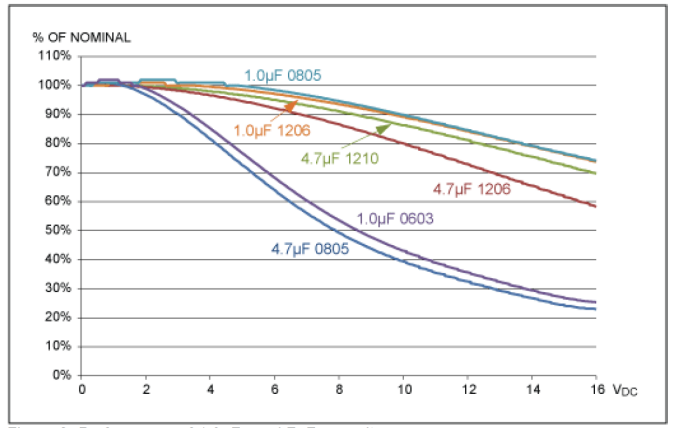
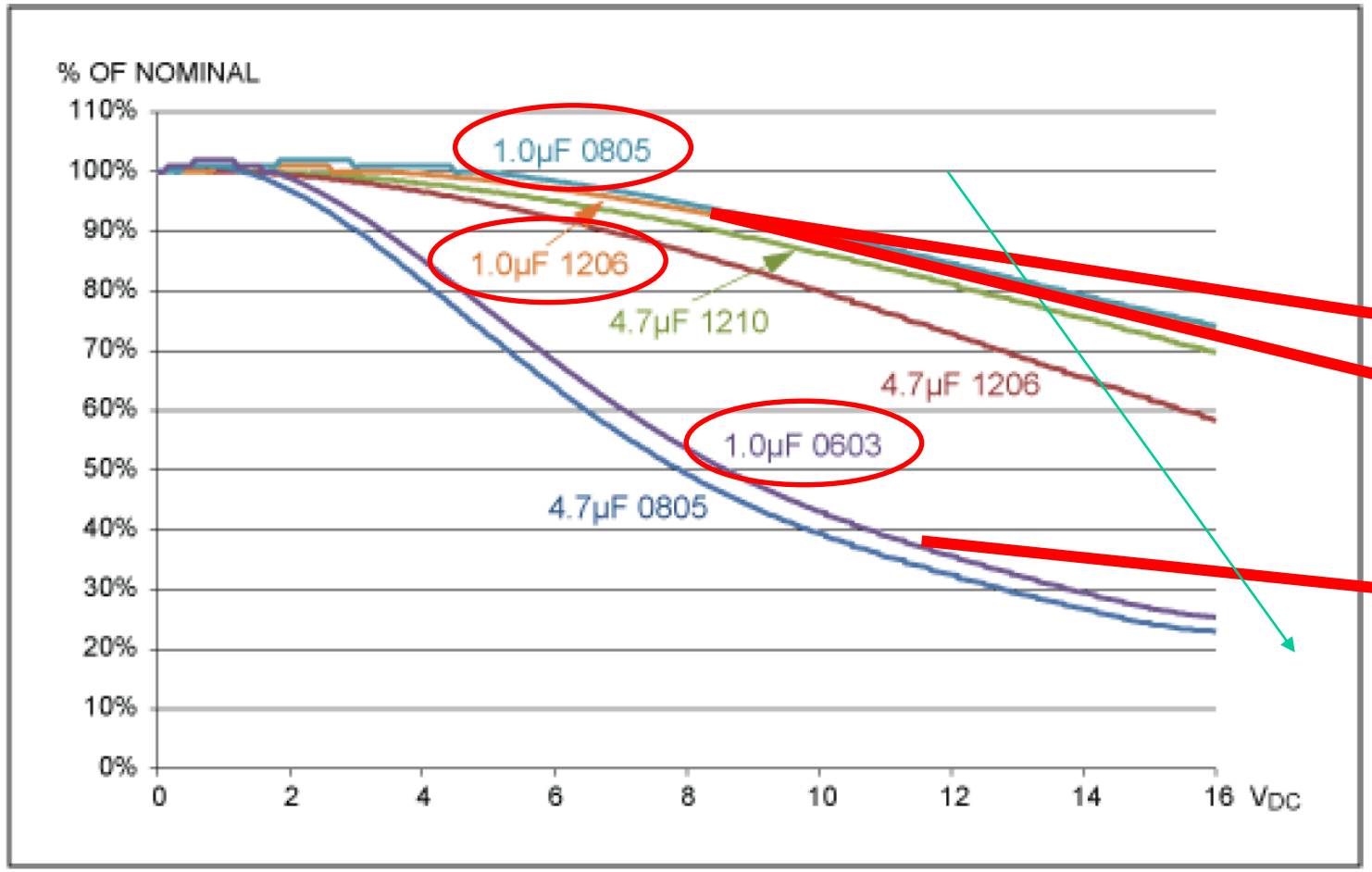


Figure 2. Performance of 1.0µF vs. 4.7µF capacitors.

The effect of size

voltage behavior of several 16V, 1.0µF X7R caps versus their 4.7µF, 16V, X7R cousins.



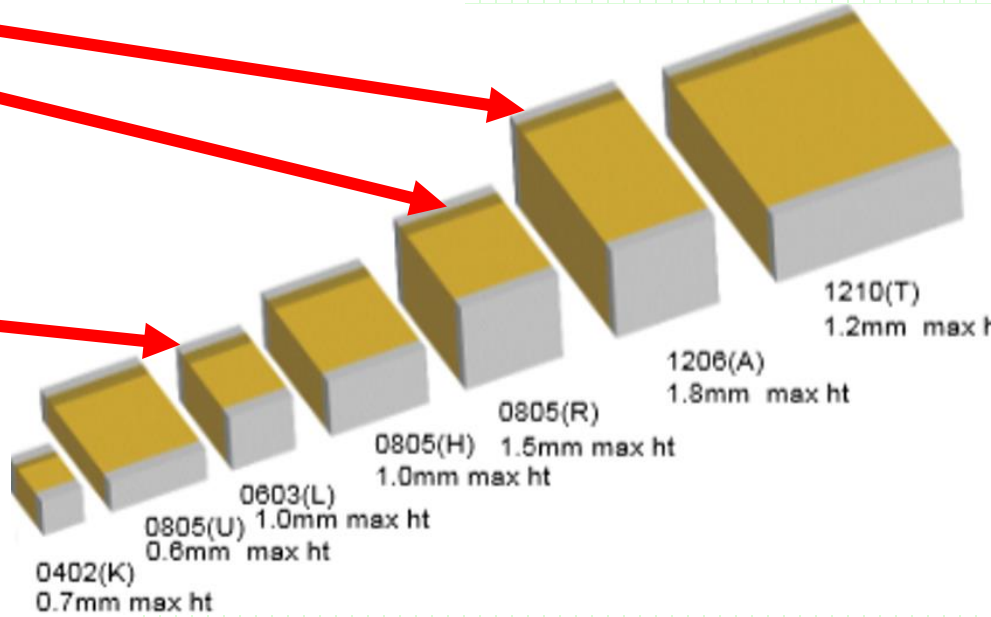


Figure 2. Performance of 1.0µF vs. 4.7µF capacitors.

The effect of size and WDCV

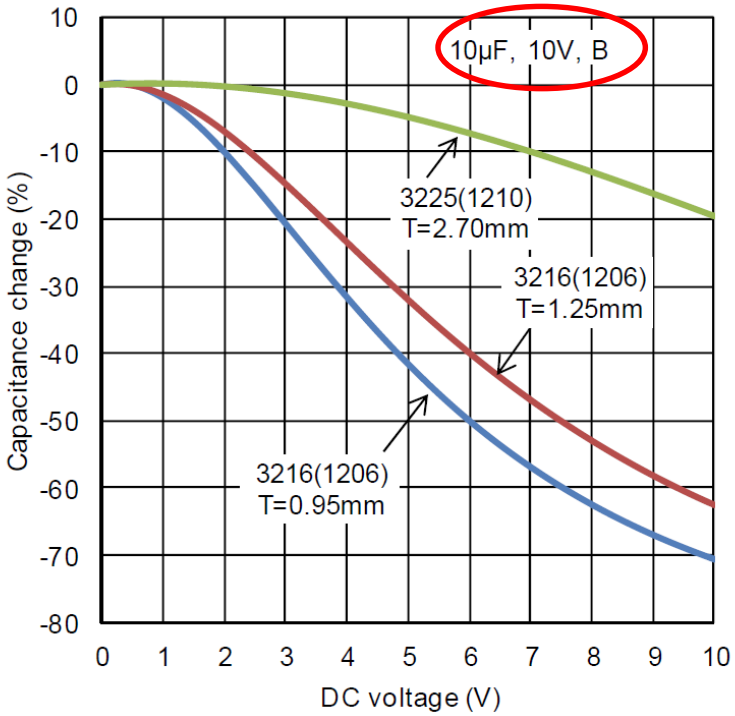


Figure 4. DC voltage characteristics
Difference in thickness (T)

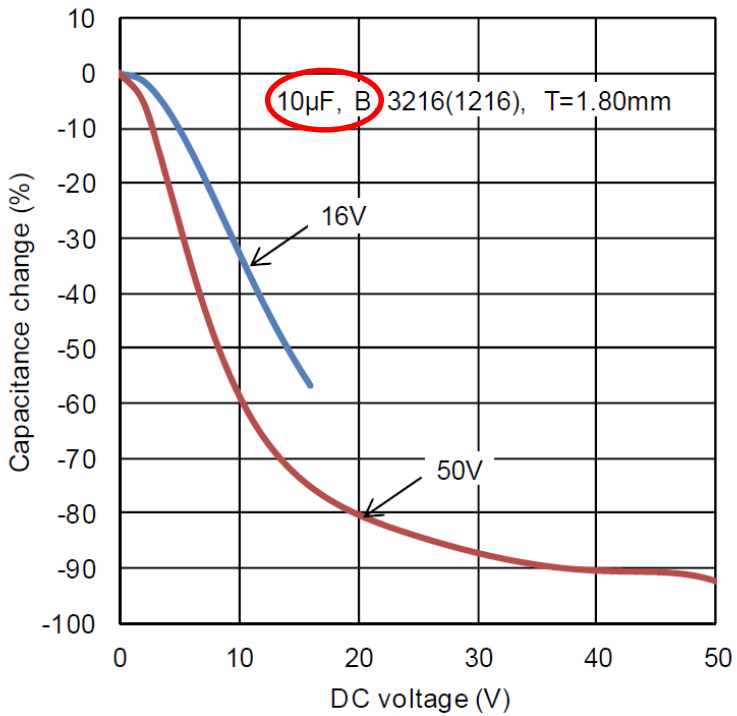
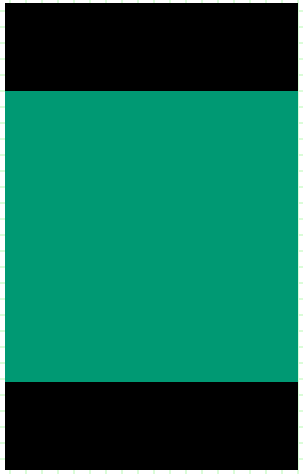
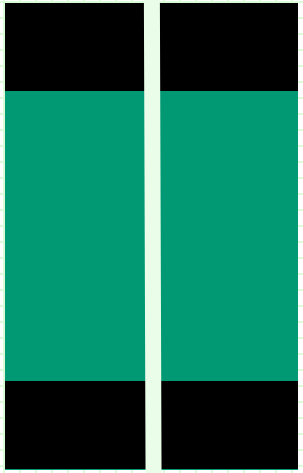


Figure 5. DC voltage characteristics
Difference in Rated-voltage

ESR as a function of bias voltage



C, ESR

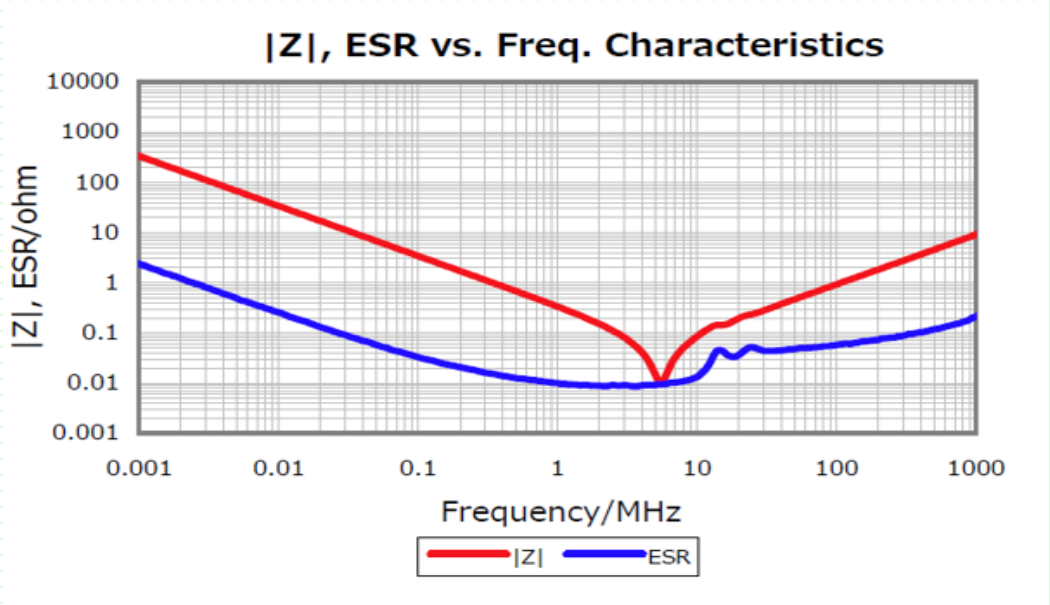


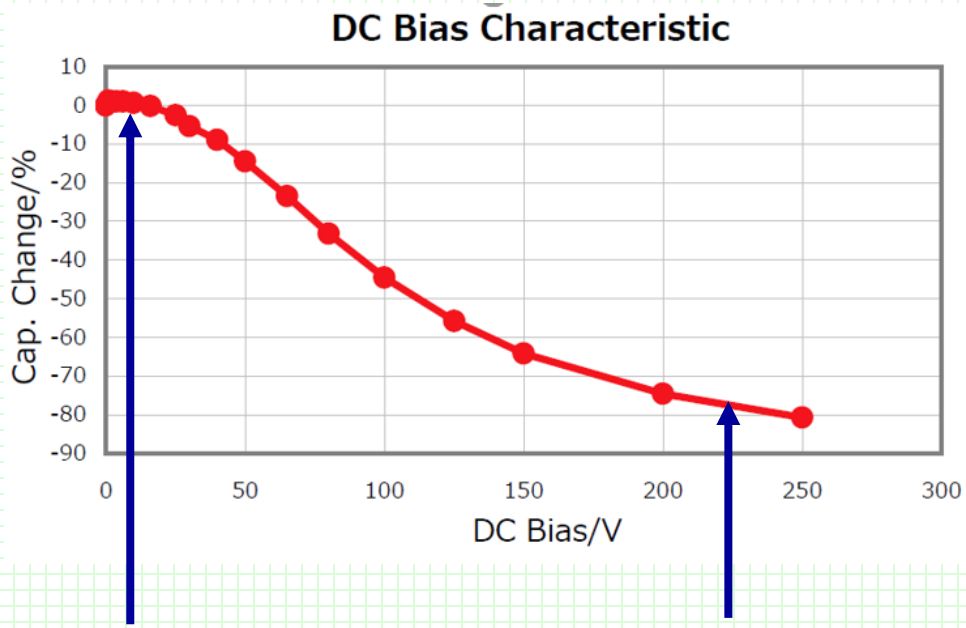
C_1, ESR_1 C_2, ESR_2

$C_1, C_2 < C$

$ESR_1, ESR_2 > ESR$

?



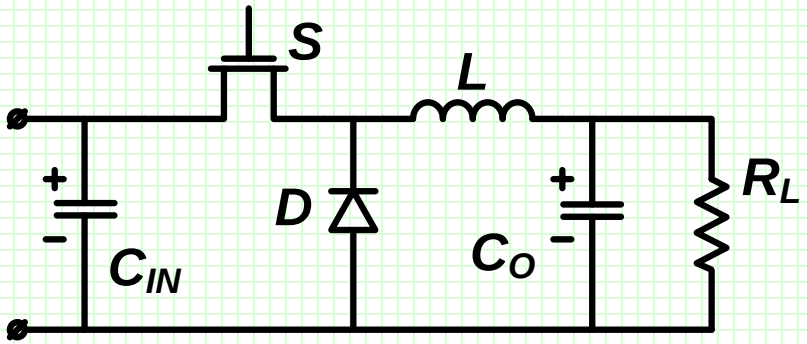


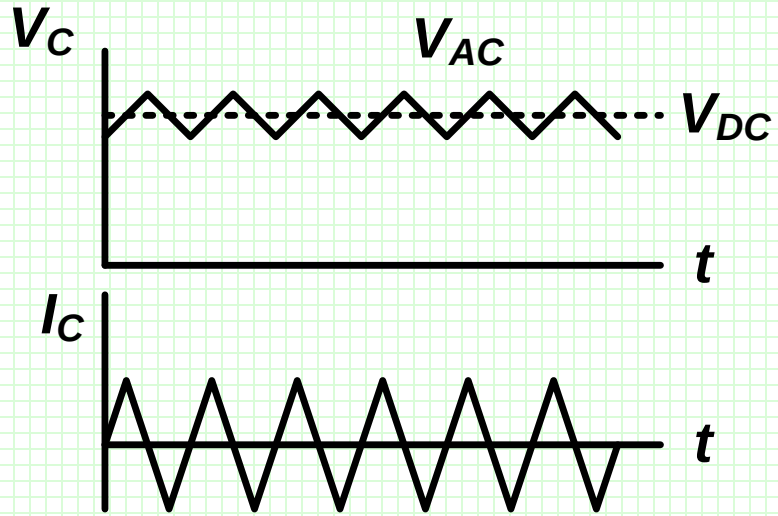
Large capacitance
Smaller ESR?

Small capacitance
Larger ESR?

Significant question because ceramic capacitors losses are:

$$P = ESR \cdot i_{rms}^2$$





Proc. of the 2014 International Symposium on Electromagnetic Compatibility (EMC Europe 2014), Gothenburg, Sweden, September 1–4, 2014

Wideband Impedance Characterization and Modeling of Power Electronic Capacitors under High Bias Voltage Variation

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[2]Embedded Electronic Systems Research Institute, IRSEEM-ESIGELEC, Saint Etienne du Rouvray, France.
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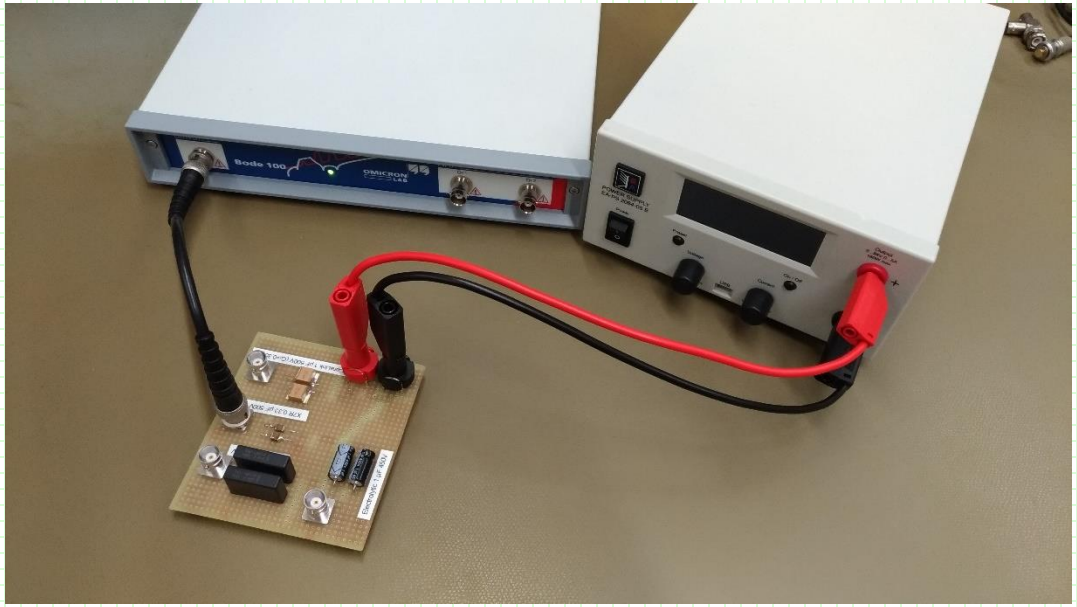
With DC bias

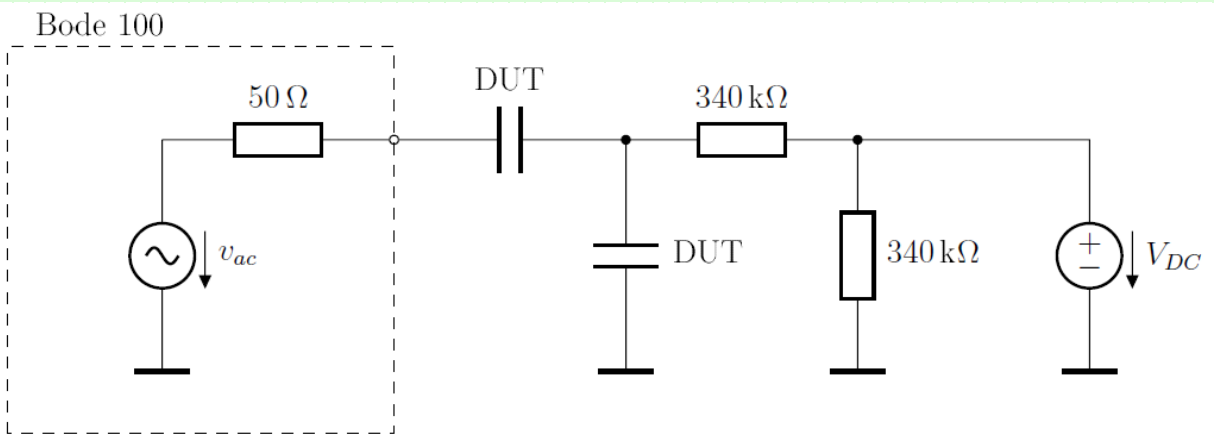
Without DC bias

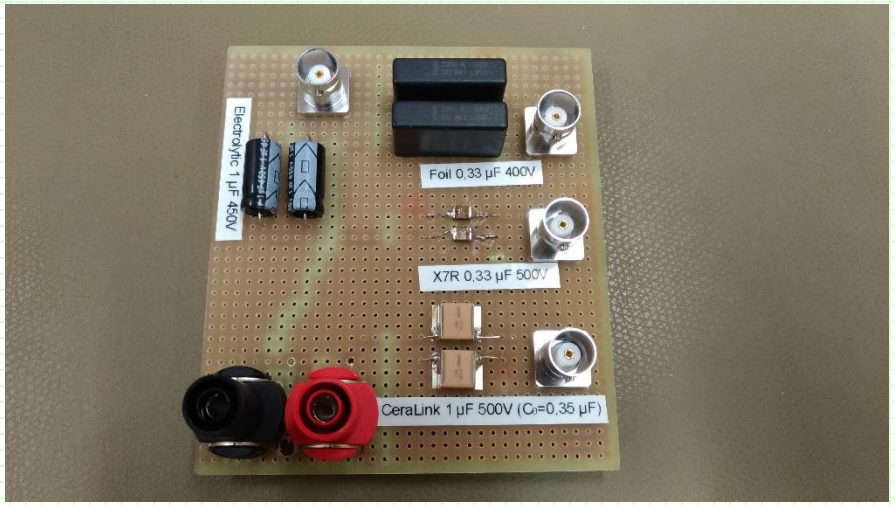
Z5U

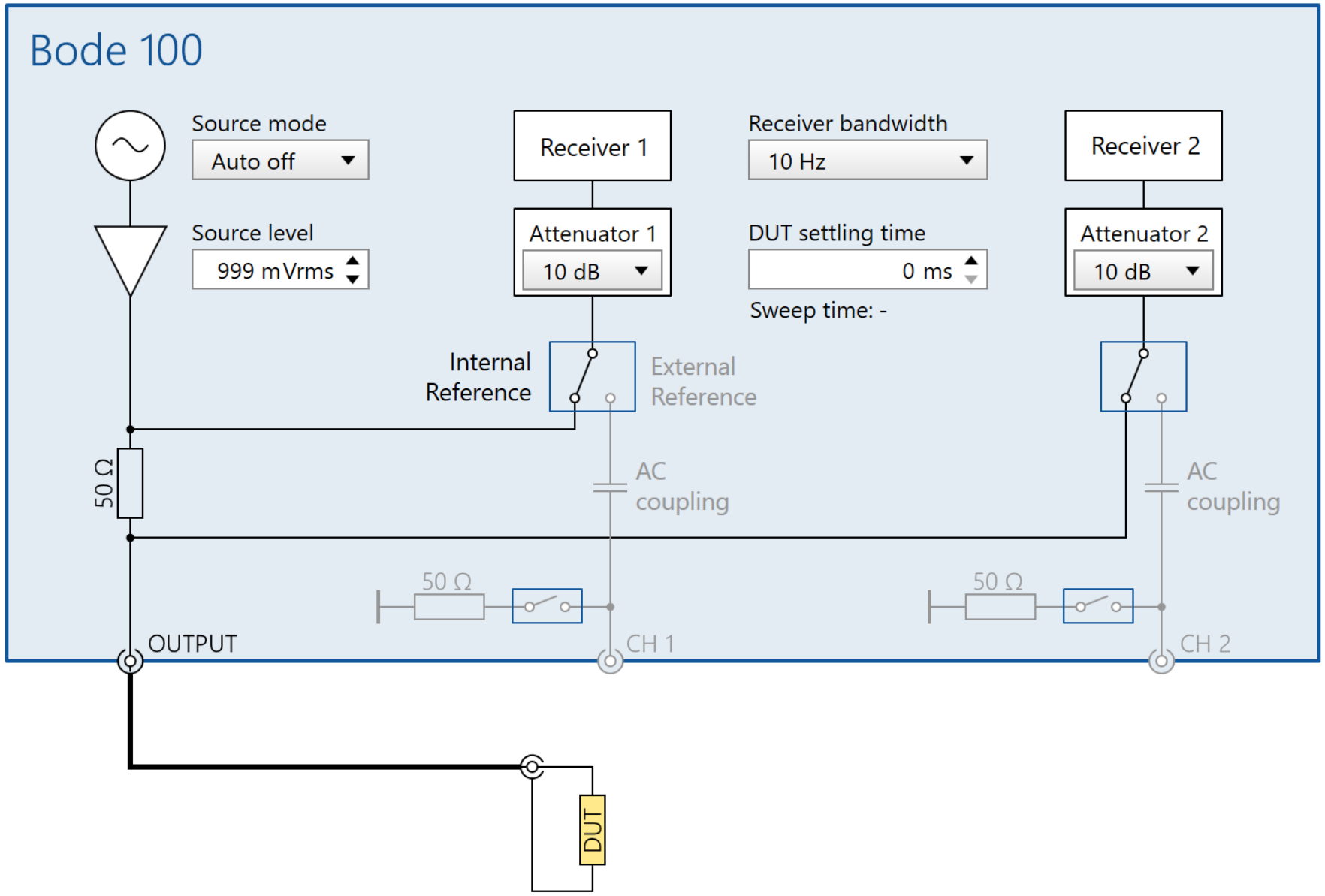
Figure 7. High frequency electric model of Z5U ceramic capacitor under applied DC bias voltage V_{rated} (a) and without the applied DC bias voltage (b).

Measurements
by Mr. Hermann Haag of Omicron LAB,
and Vorarlberg University of Applied Sciences, Austria
using Omicron's Bode 100 Network Analyzer

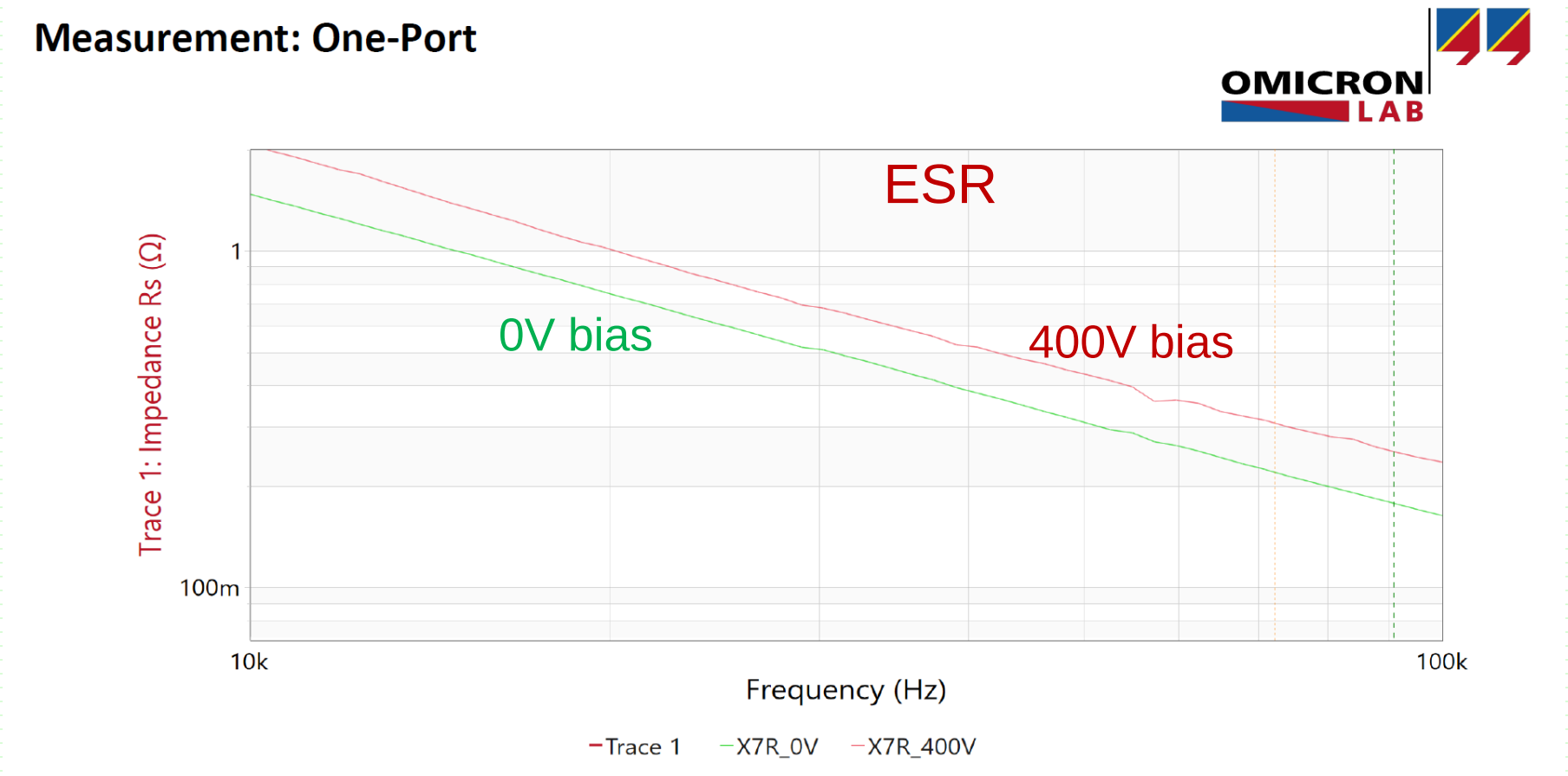







Bode 100
Source mode
Auto off
Source level
999 mVrms
Receiver 1
Attenuator 1
10 dB
Receiver bandwidth
10 Hz
DUT settling time
0 ms
Sweep time: -
Receiver 2
Attenuator 2
10 dB
Internal Reference
External Reference
50 Ω
AC coupling
AC coupling
50 Ω
50 Ω
OUTPUT
CH 1
CH 2
DUT

According to Bode 100 measurements ESR is increasing with bias
(consistent with paper)



C1812W334KCRACTU (same as K-SIM data)

2016 IEEE 36th International Conference on Electronics and Nanotechnology (ELNANO)

Specifics of the X7R Capacitors Application in the High Frequency Inverters

Alexey Tyshko
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Saulius Balevicius
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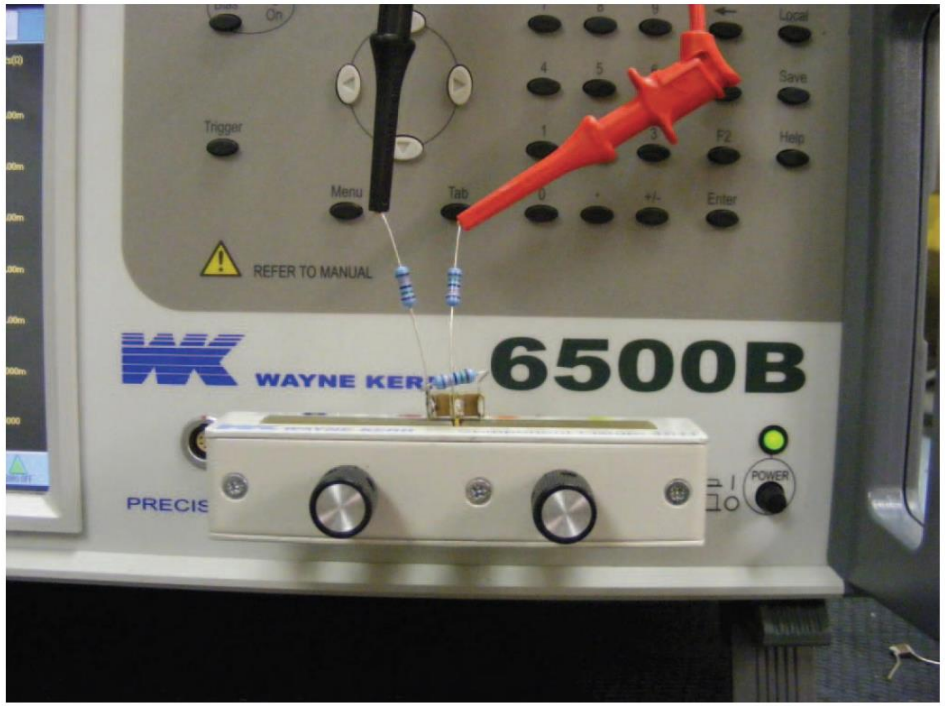
sbal@pfi.lt



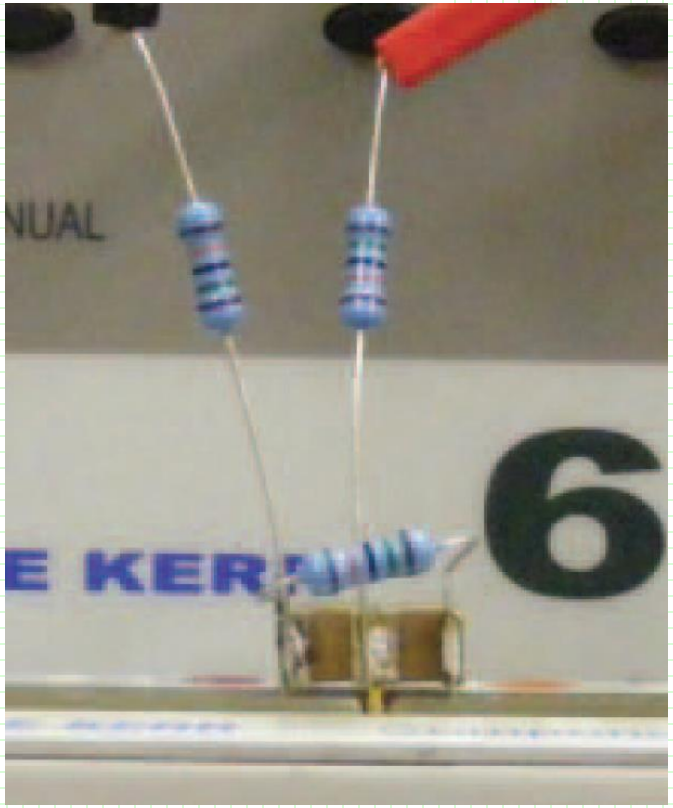


Fig. 4. Capacitor test setup

CKG57NX7R2A106M500JH

TDK Item Description : CKG57NX7R2A106MT****

Lead Free | Halogen Free | REACH | RoHS COMPLIANT

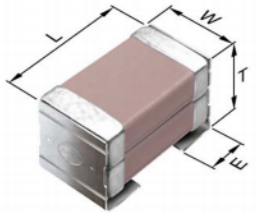
Characterization Sheet (Multilayer Ceramic Chip Capacitors)

Application & Main Feature

Commercial Grade (MEGACAP Type)

Series

CKG57N(5750) [EIA CC2220]



Dimensions

L	6.00mm +/-0.5mm
W	5.00mm +/-0.5mm
T	5.00mm +/-0.5mm
E	1.60mm +/-0.3mm

Temperature Characteristic

X7R (-55 to 125 degC +/-15%)

Rated Voltage

2A (100Vdc)

Capacitance

10uF

Capacitance Tolerance

M (+/-20%)

Dissipation Factor

3% Max.

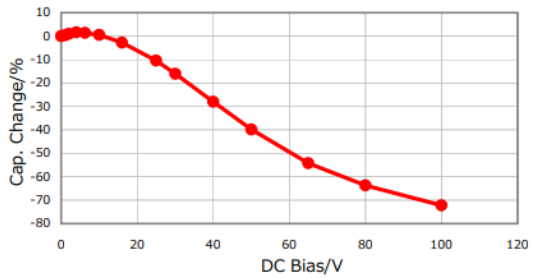
Insulation Resistance

50Mohm Min.

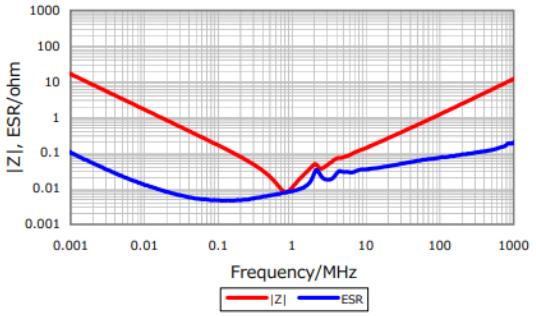
AEC-Q200

Not Applicable

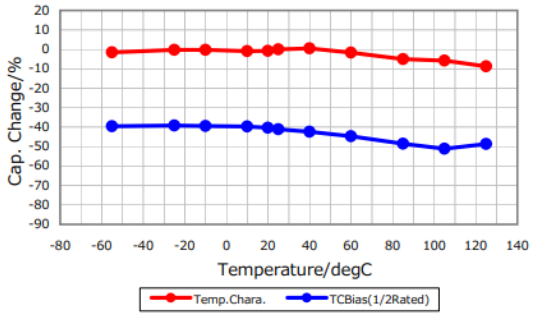
DC Bias Characteristic



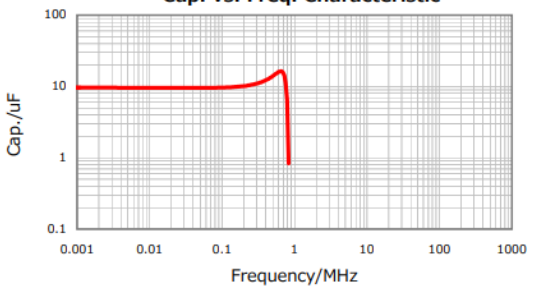
|Z|, ESR vs. Freq. Characteristics



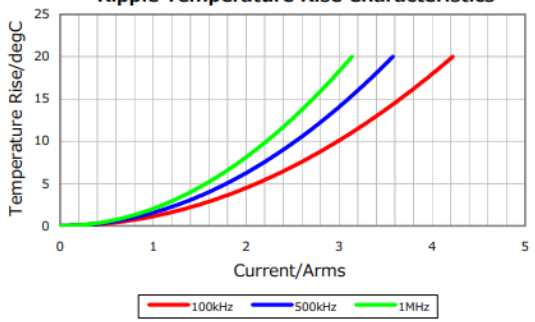
Temperature Characteristics



Cap. vs. Freq. Characteristic



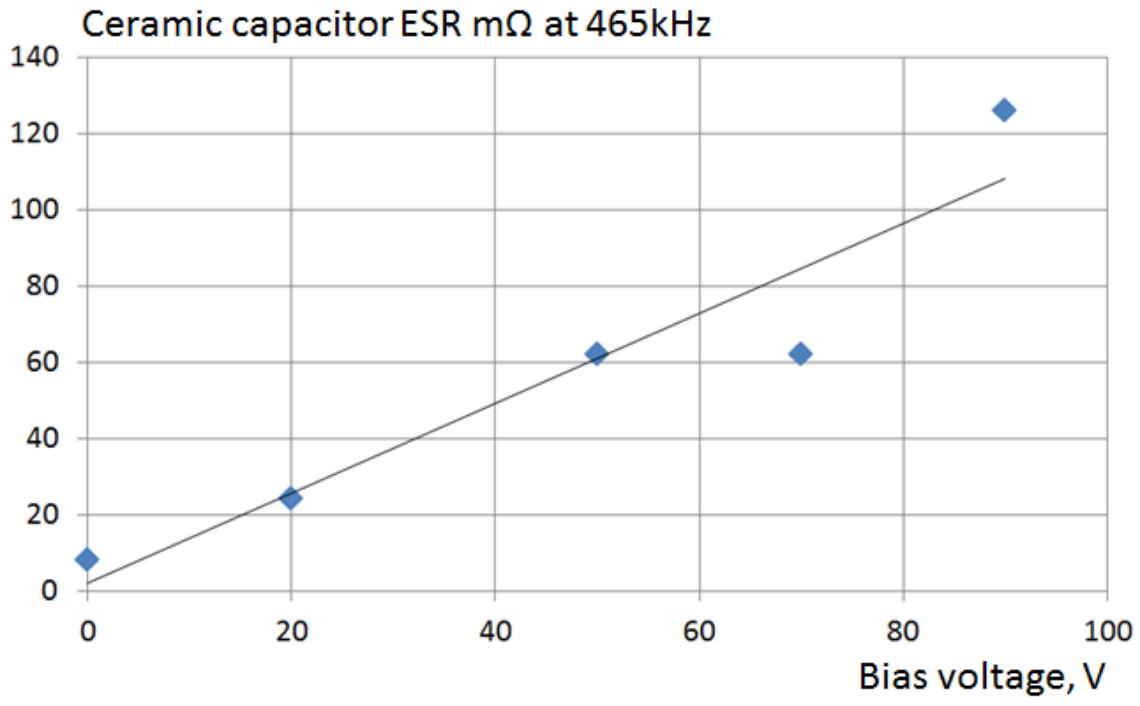
Ripple Temperature Rise Characteristics



TDK

All specifications are subject to change without notice.

January 4, 2016



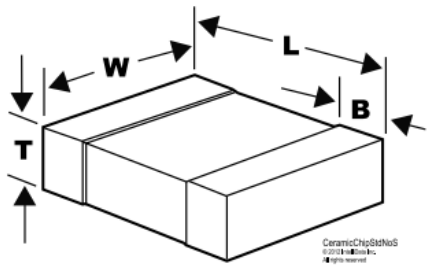
80V bias increases ripple current loss by more then 10 fold!

???

KEMET Part Number: C1812W334KCRACTU
(C1812W334KCRAC7800)

Electronic Components KEMET CHARGED.

Ceramic, Anti-Arcing, ArcShieldFlexTerm-(CxxxxW), 0.33 uF, 10%, 500 V, 1812, X7R, SMD, MLCC, Arcshield, High Voltage



General Information	
Style:	SMD Chip
Series:	ArcShieldFlexTerm-(CxxxxW)
Chip Size:	1812
Description:	SMD, MLCC, Arcshield, High Voltage
Features:	High Voltage
RoHS:	Yes
Termination:	Flexible Termination
Marking:	No
Failure Rate:	N/A
Miscellaneous:	Note: Referee time for X7R dielectric for this part number is 1000 hours. X7R dielectric is not recommended for AC line filtering or pulse applications

Dimensions	
L	4.5mm +/-0.4mm
W	3.2mm +/-0.3mm
T	2.1mm +/-0.20mm
B	0.7mm +/-0.35mm

Packaging Specifications	
Packaging:	T&R, 180mm, Plastic Tape
Packaging Quantity:	500

Specifications	
Capacitance:	0.33 uF
Capacitance Tolerance:	10%
Voltage DC:	500 VDC
Dielectric Withstanding Voltage:	750 V
Temperature Range:	-55/+125C
Temperature Coefficient:	X7R
Dissipation Factor:	2.5%
Aging Rate:	3% Loss/Decade Hour
Insulation Resistance:	303 MOhms

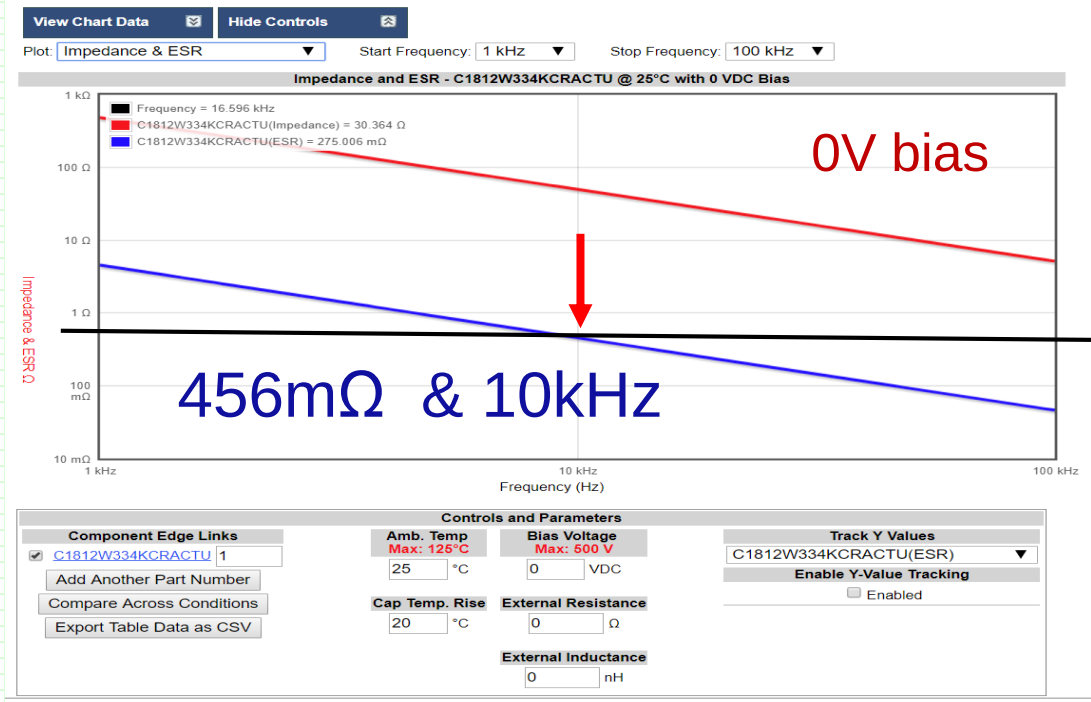
X7R
0.33uF
500V
1812

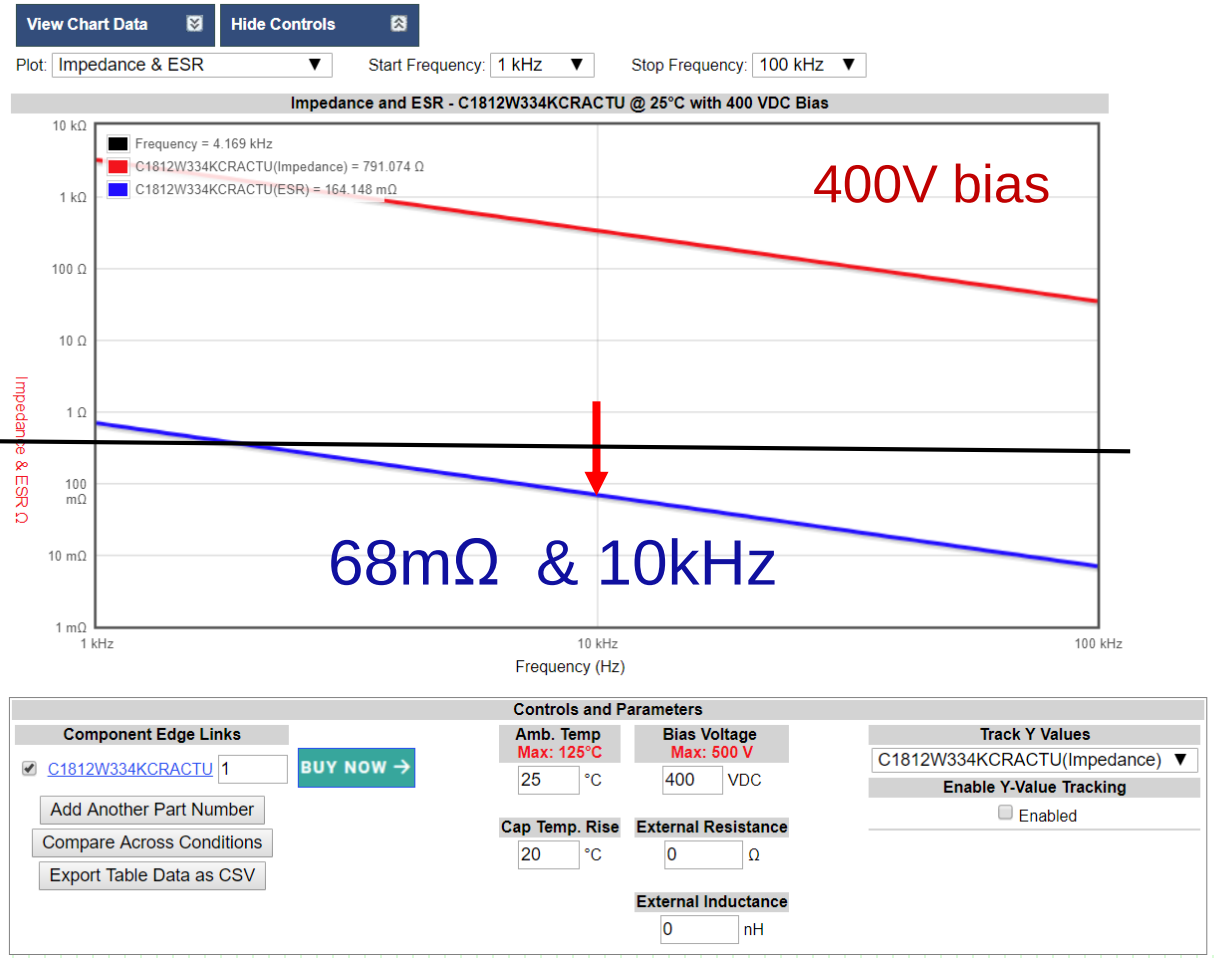
Same as the one tested by Bode 100

K-SIM KEMET


View Chart Data
Hide Controls
Plot: Impedance & ESR
Start Frequency: 1 kHz
Stop Frequency: 100 MHz
Impedance and ESR - C1812W334KCRACTU @ 25°C with 0 VDC Bias
Frequency = 95.499 kHz
C1812W334KCRACTU(Impedance) = 5.404 Ω
C1812W334KCRACTU(ESR) = 48.217 mΩ
Z
ESR
1 kΩ
100 Ω
10 Ω
1 Ω
100 mΩ
10 mΩ
1 mΩ
100 µΩ
Impedance & ESR Ω
1 kHz
10 kHz
100 kHz
1 MHz
10 MHz
100 MHz
Frequency (Hz)
Controls and Parameters
Component Edge Links
C1812W334KCRACTU 1
Add Another Part Number
Compare Across Conditions
Export Table Data as CSV
Amb. Temp
Max: 125°C
25 °C
Bias Voltage
Max: 500 V
0 VDC
Cap Temp. Rise
20 °C
External Resistance
0 Ω
External Inductance
0 nH
Track Y Values
C1812W334KCRACTU(Impedance)
Enable Y-Value Tracking
Enabled

According to K-SIM ESR is decreasing with bias (not consistent with papers and Bode100 results)





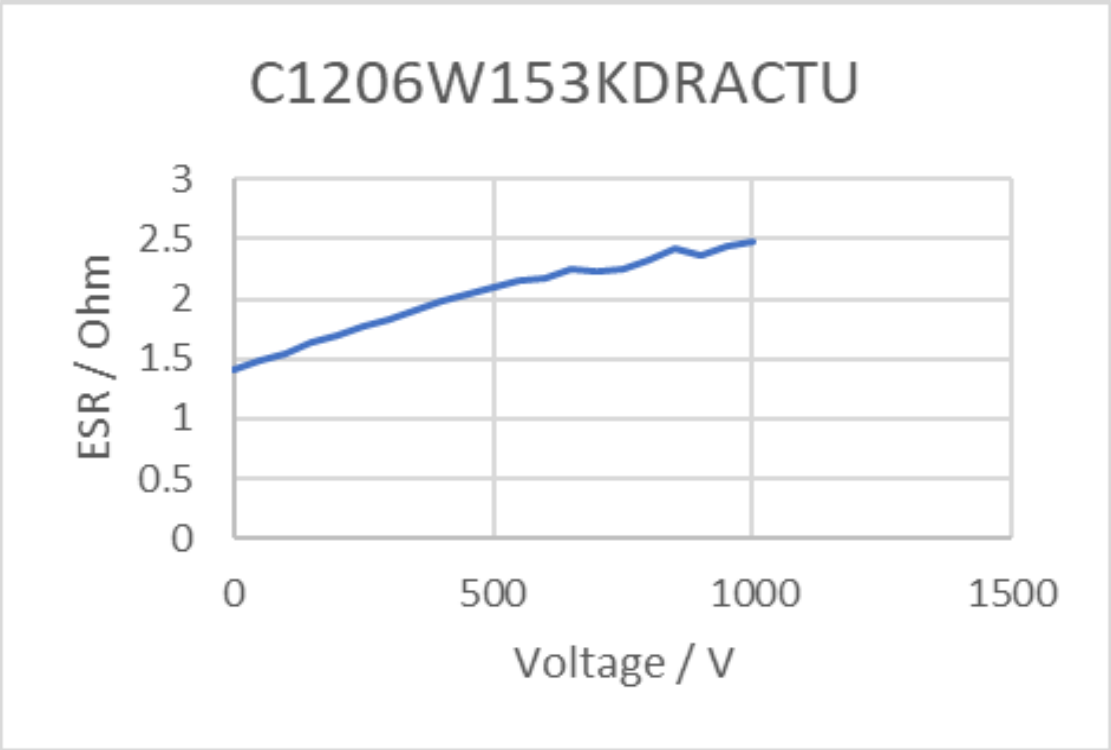
?

Submitted to PCIM- 2020

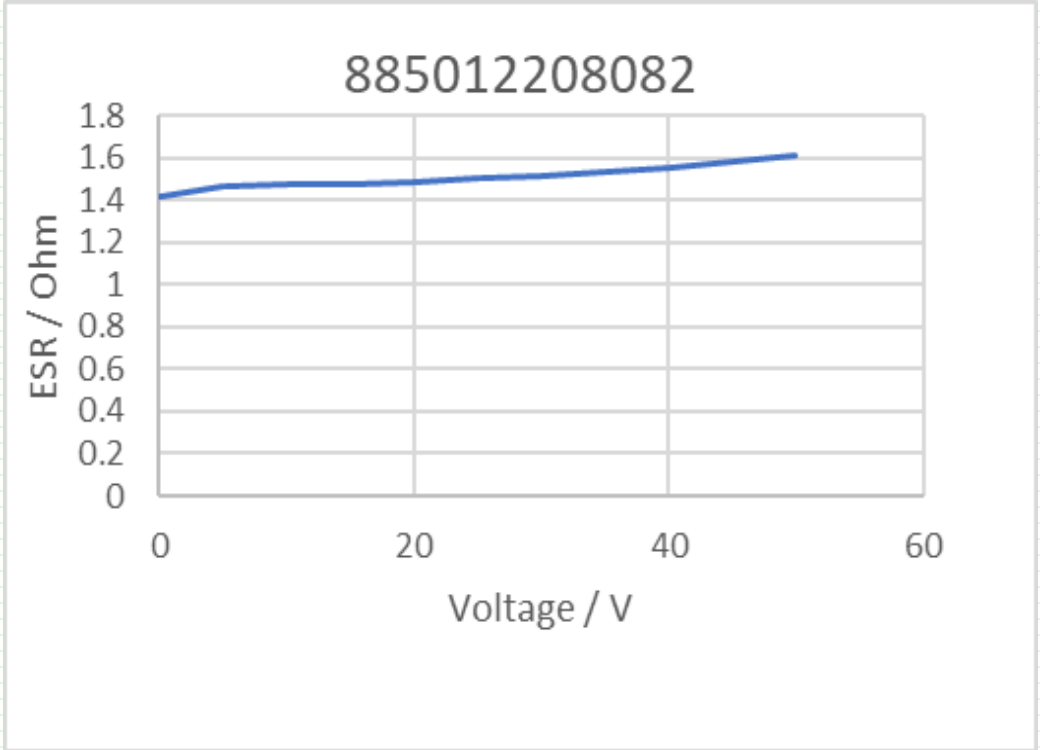
Voltage bias effect on the ESR of ferroelectric ceramic capacitors

Hermann Haag[1], Florian Hämmerle[1], and Shmuel (Sam) Ben-Yaakov[2]

[1] Omicron Lab, Austria
[2] Ben-Gurion University, Israel



X7R, 15nF, 1000V capacitor
(KEMET, C1206W153KDRACTU),



X7R, 15nF, 50V capacitor
(Wurth, 885012208082).

Table I. A summary of measured ESR and comparison to K-SIM simulation

Material	Capacitance		Voltage	ESR change	ESR K-SIM
X5R	3.3µF		25V	+25.1%	-68.0%
X5R	10µF		25V	+30.5%	
X5R	47µF		16V	+1.2%	
X7R	330nF		50V	+20.4%	-20.0%
X7R	2.2µF		50V	+64.8%	
X7R	15nF		50V	+13.7%	
X7R	15nF		1000V	+76.3%	
X7R	68nF		1000V	+71.1%	

Piezoelectricity

1. Ferroelectric dielectric is piezoelectric
2. Reciprocal relation between electrical field and mechanical stress
3. When electrically driven by AC ceramic capacitors emit acoustic waves
4. Multiple resonant frequencies
5. Can cinduce“ singing capacitors” phenomenon
5. Can be used to detect defects

Capacitors for Reduced Microphonics and Sound Emission

Mark Laps, Roy Grace, Bill Sloka, John Prymak, Xilin Xu, Pascal Pinceloup, Abhijit Gurav, Michael Randall, Philip Lessner, Aziz Tajuddin

KEMET Electronics Corporation, 201 Fairview Street Extension, Fountain Inn, SC 29644
Phone: 864-409-5629, FAX: 864-409-5642
e-mail: marklaps@kemet.com

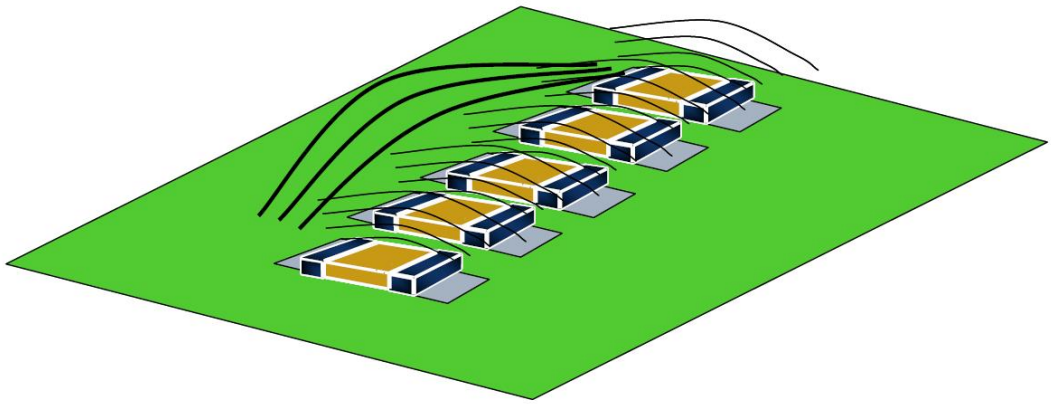


Figure 7. Capacitor distortion transferred to the PCB acting as an amplifier.

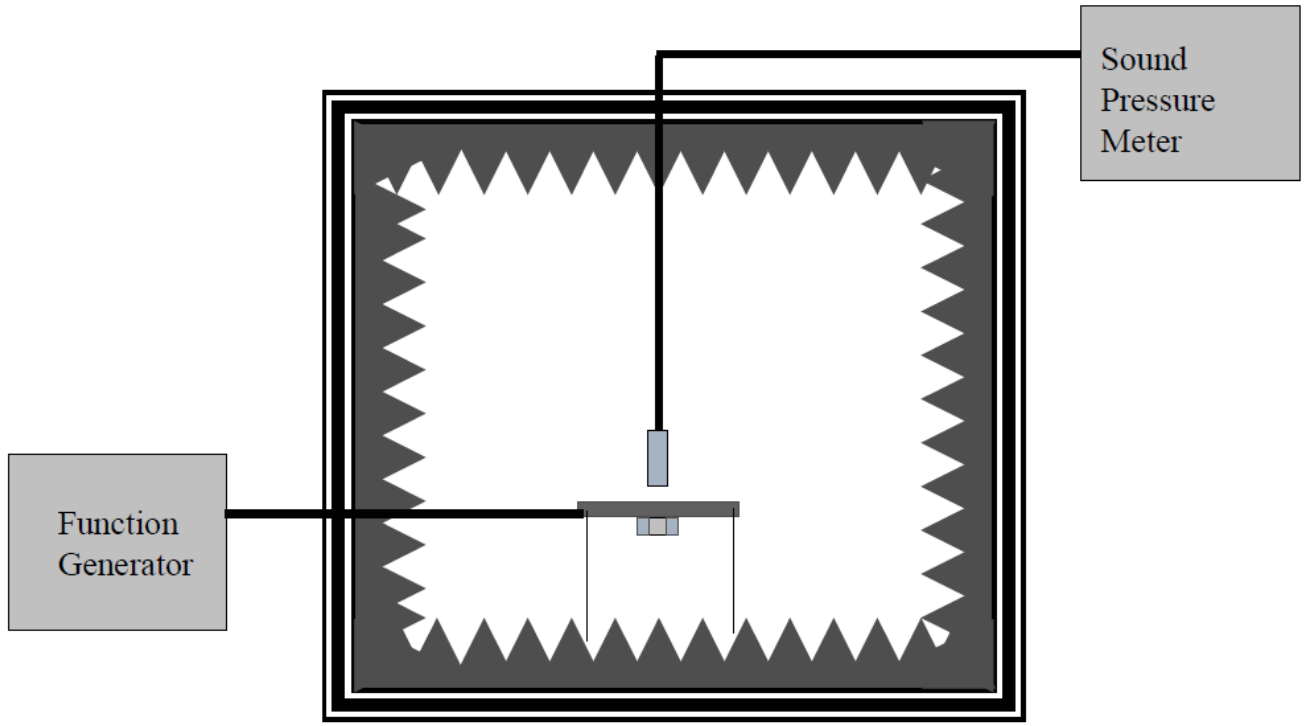
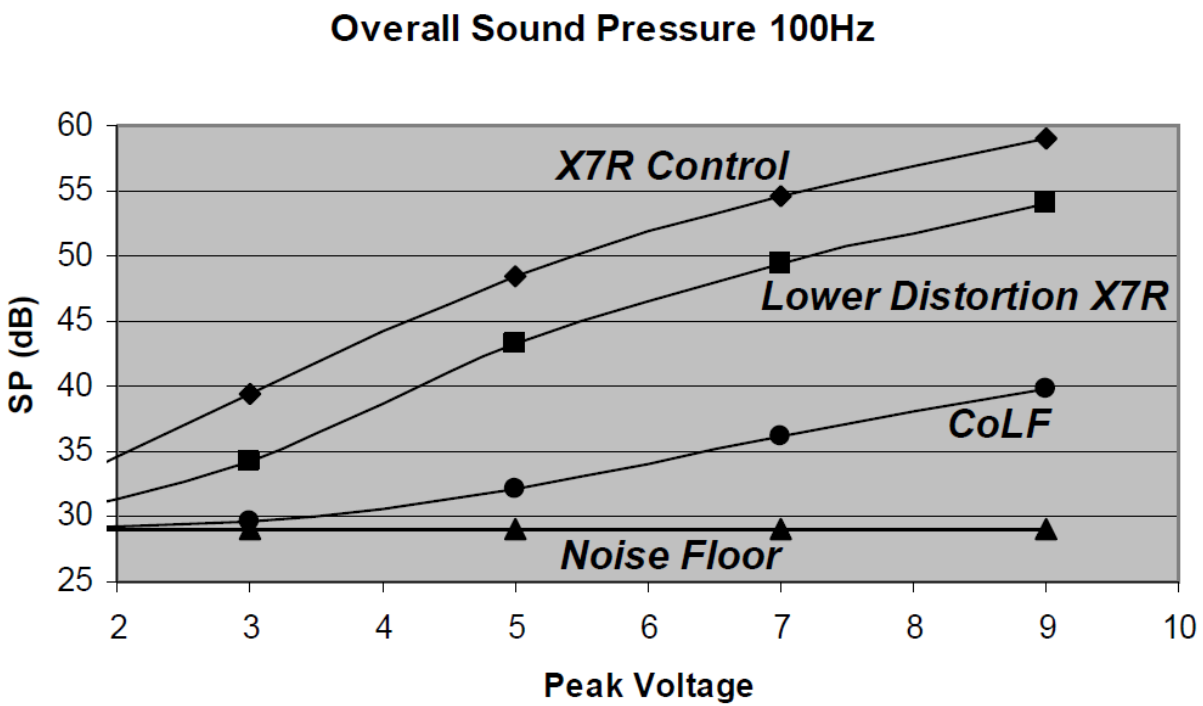
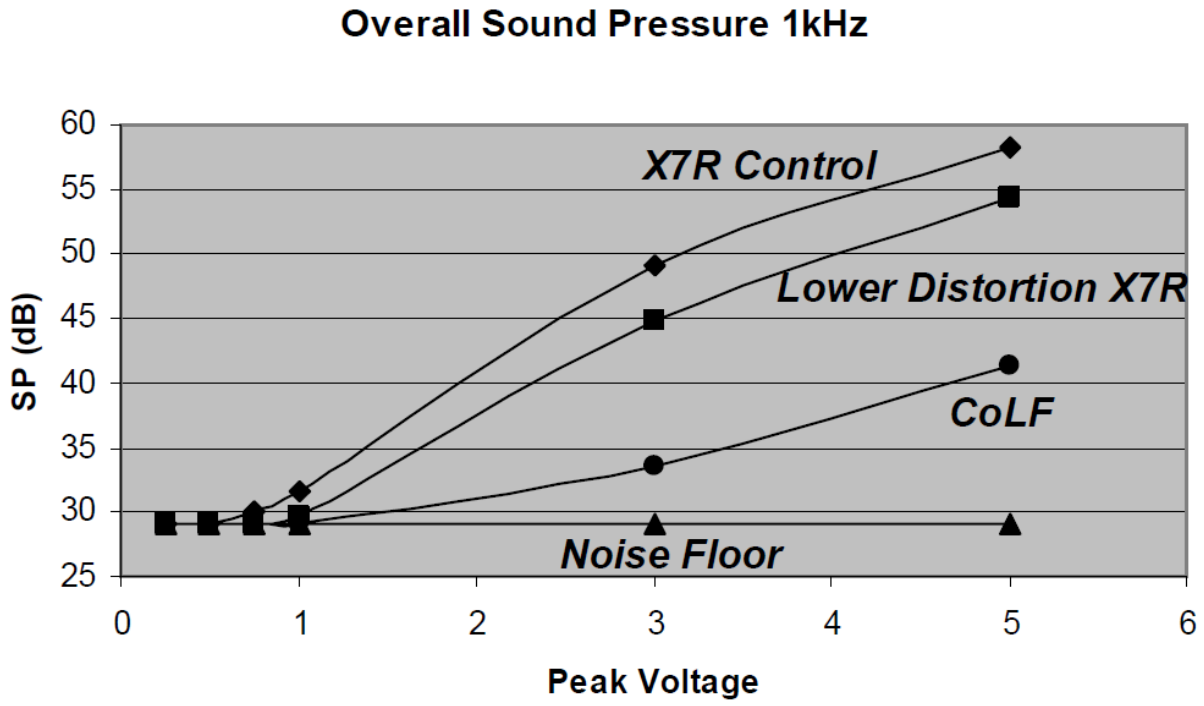


Figure 10. Setup for measuring noise performance of test samples.


Overall Sound Pressure 100Hz
X7R Control
Lower Distortion X7R
CoLF
Noise Floor
SP (dB)
Peak Voltage
60
55
50
45
40
35
30
25
2
3
4
5
6
7
8
9
10


Overall Sound Pressure 1kHz
X7R Control
Lower Distortion X7R
CoLF
Noise Floor
SP (dB)
Peak Voltage
60
55
50
45
40
35
30
25
0
1
2
3
4
5
6

2016 IEEE 36th International Conference on Electronics and Nanotechnology (ELNANO)

Specifics of the X7R Capacitors Application in the High Frequency Inverters

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Center of Physical Sciences and Technology and
Vilnius Gediminas Technical University
Vilnius, Lithuania
sbal@pfi.lt

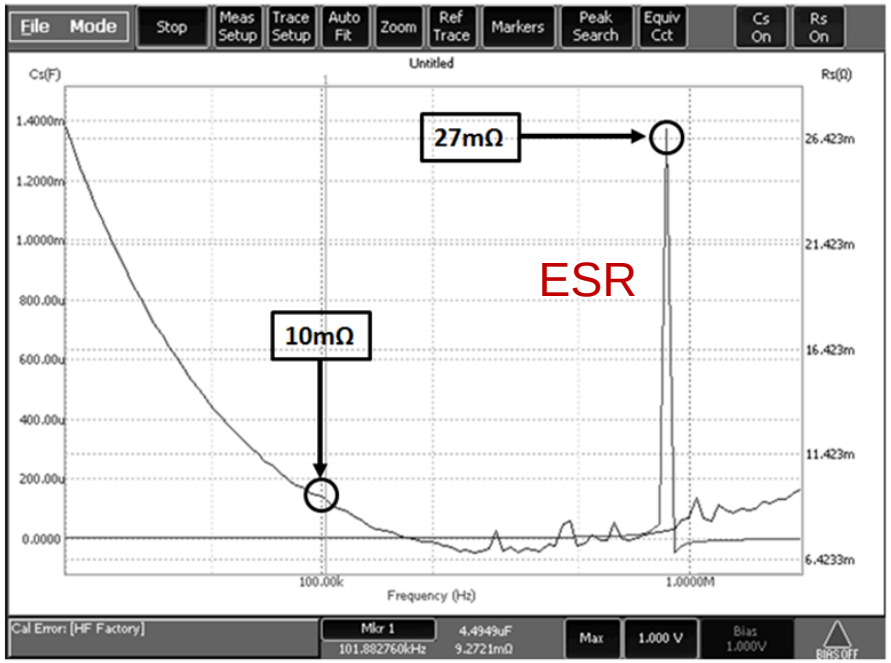
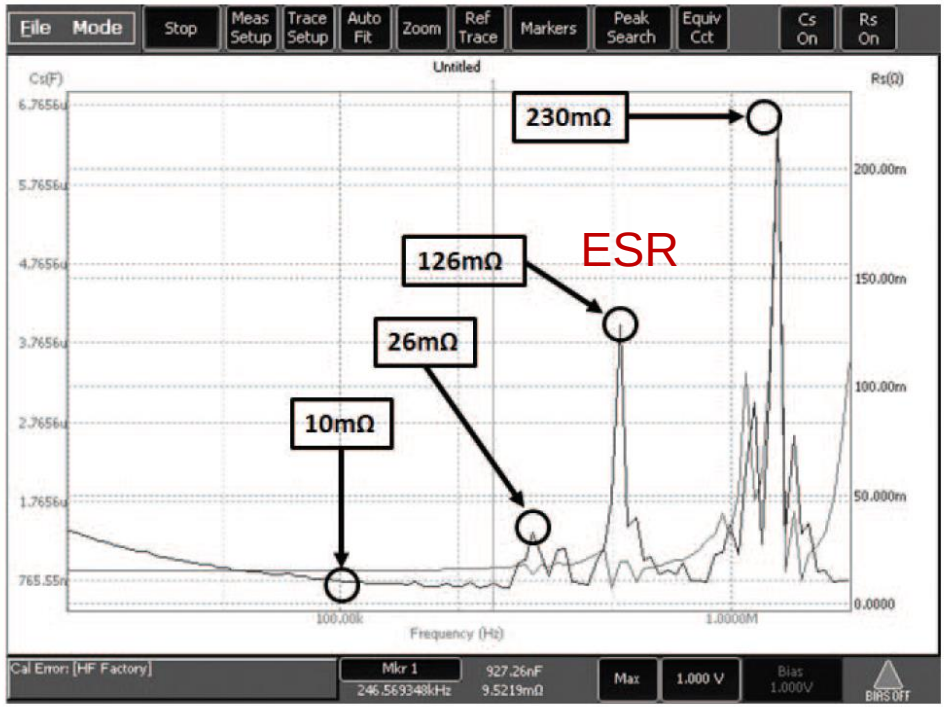
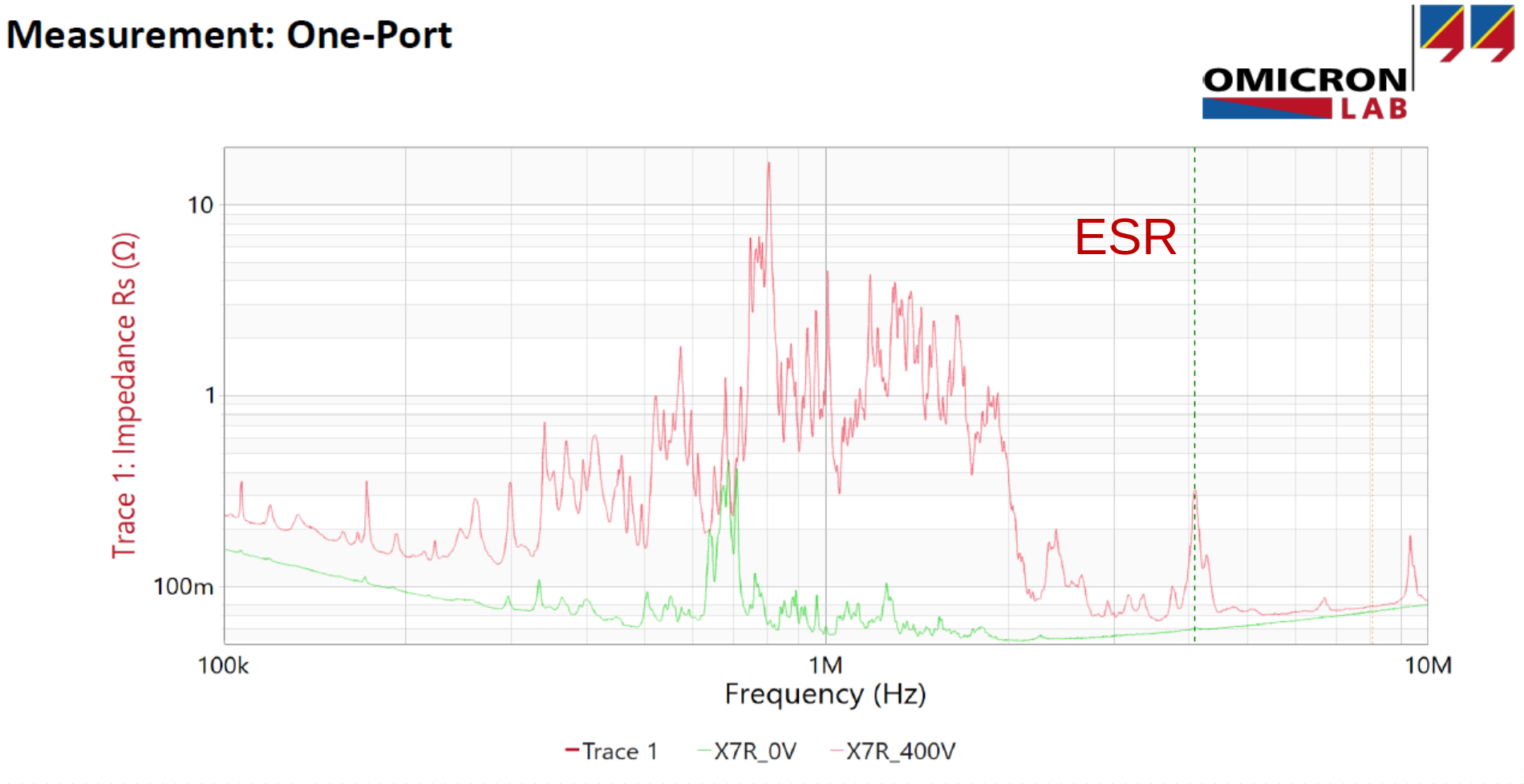


Figure 6 Frequency scan of the capacitance and ESR.

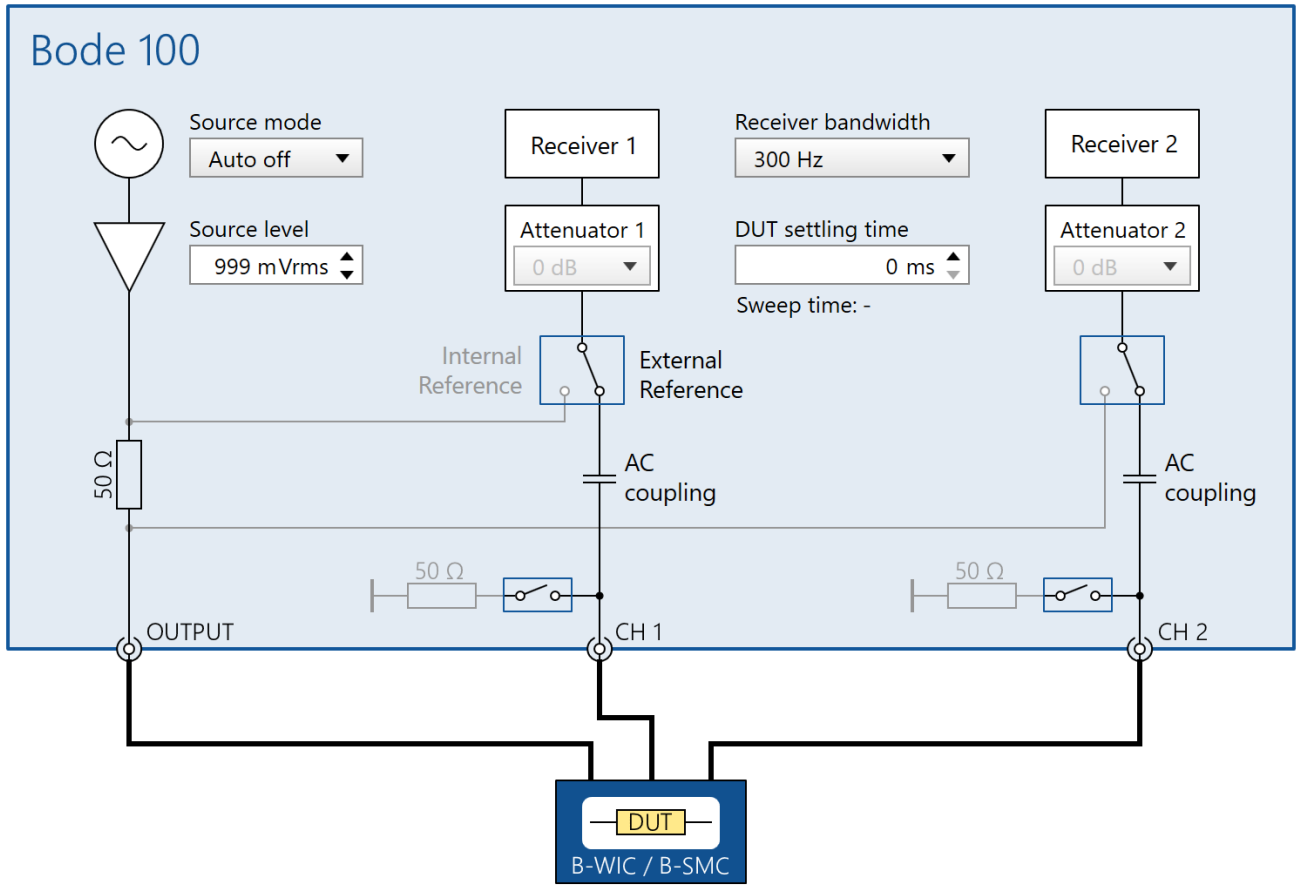


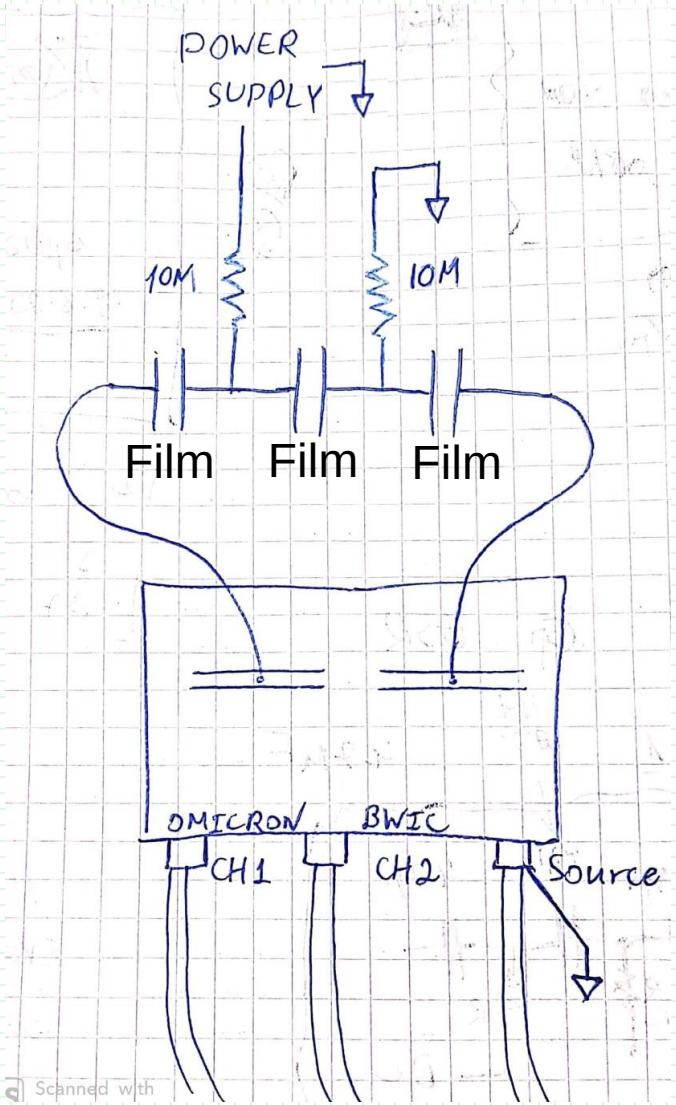
Measurements
by Mr. Hermann Haag of Omicron LAB,
and Vorarlberg University of Applied Sciences,
using Omicron's Bode 100 Network Analyzer



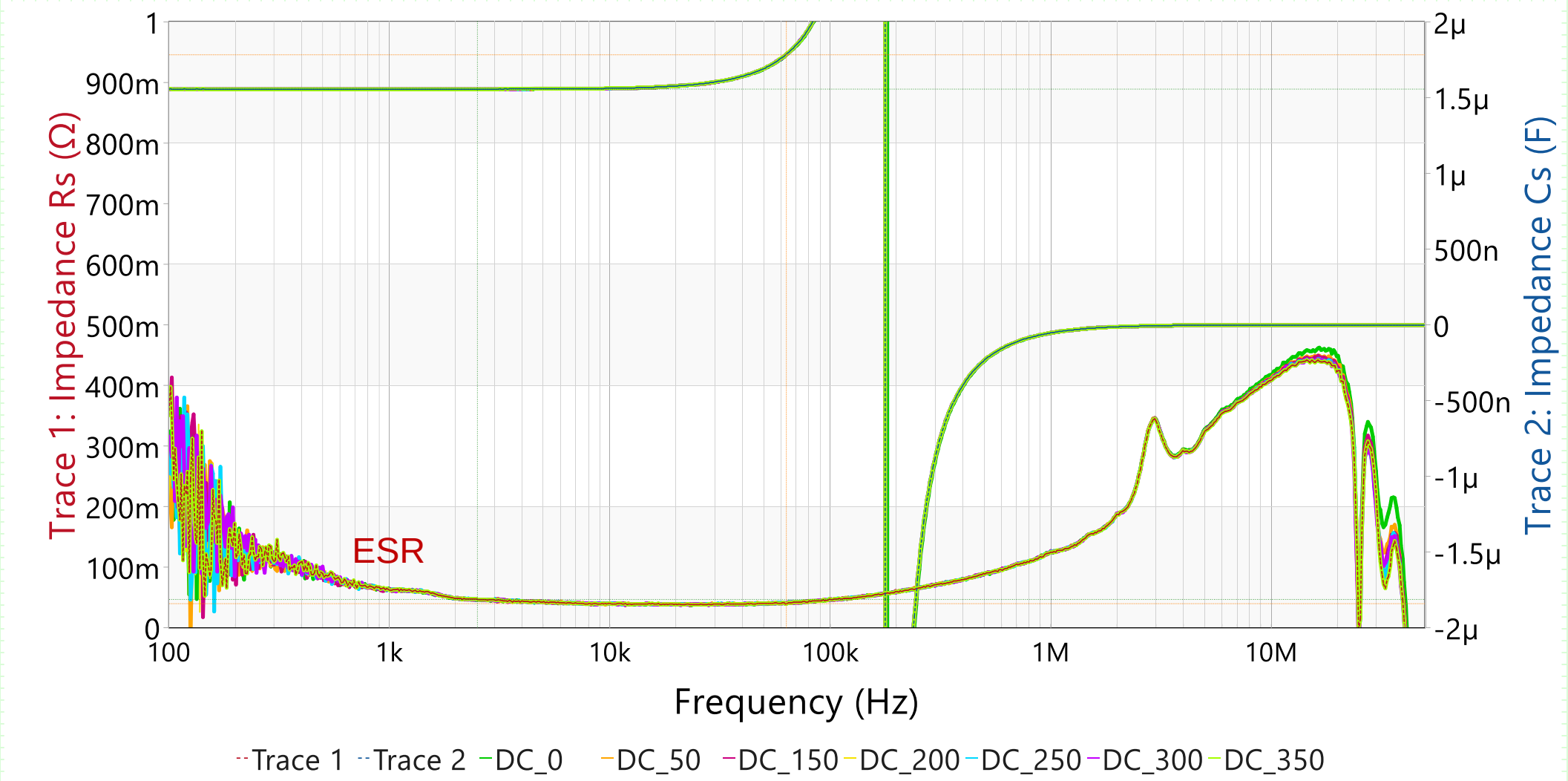
Experiment Setup for Film Capacitor

Measurements
by Mr. Stanislav Tishechkin, Department of ECE, Ben-Gurion University,
using Omicron's Bode 100 Network Analyzer

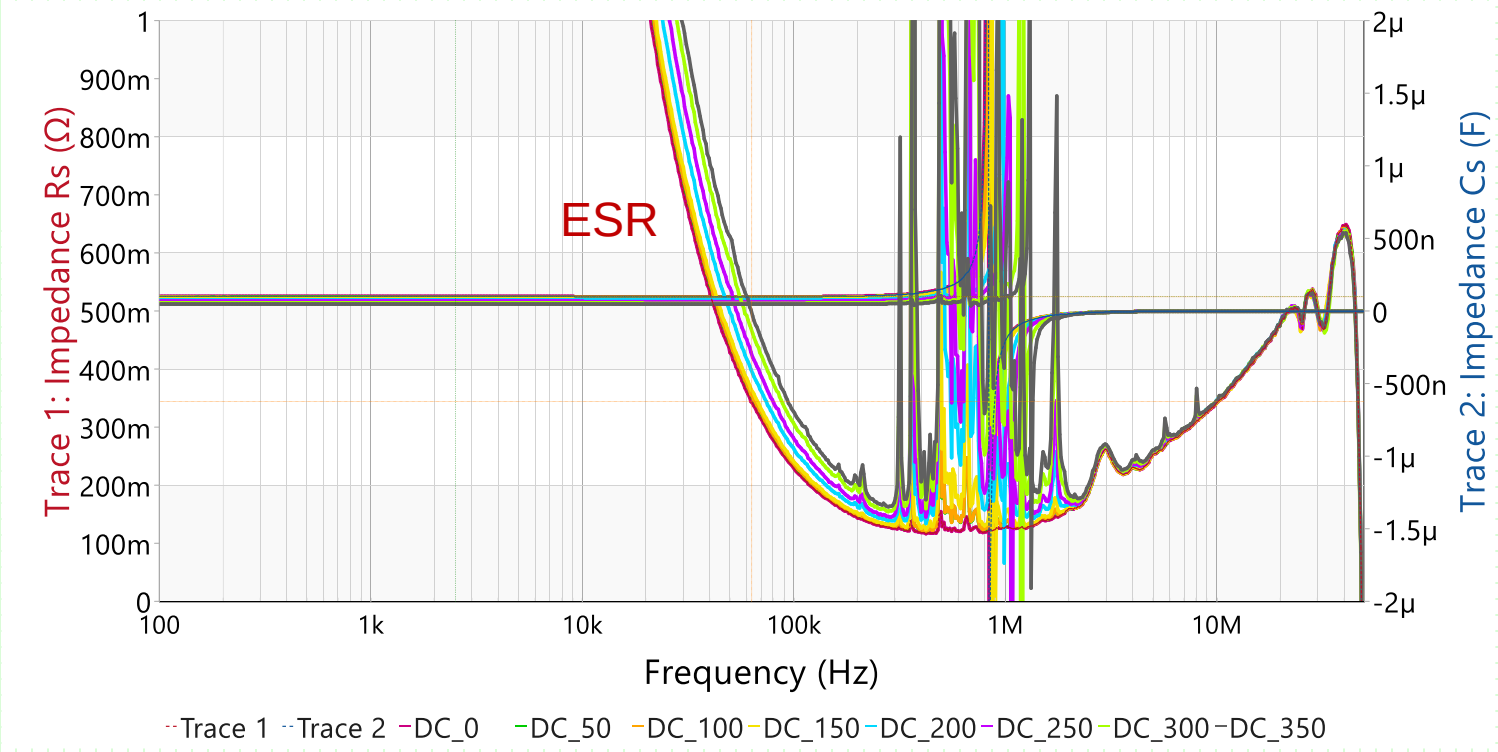


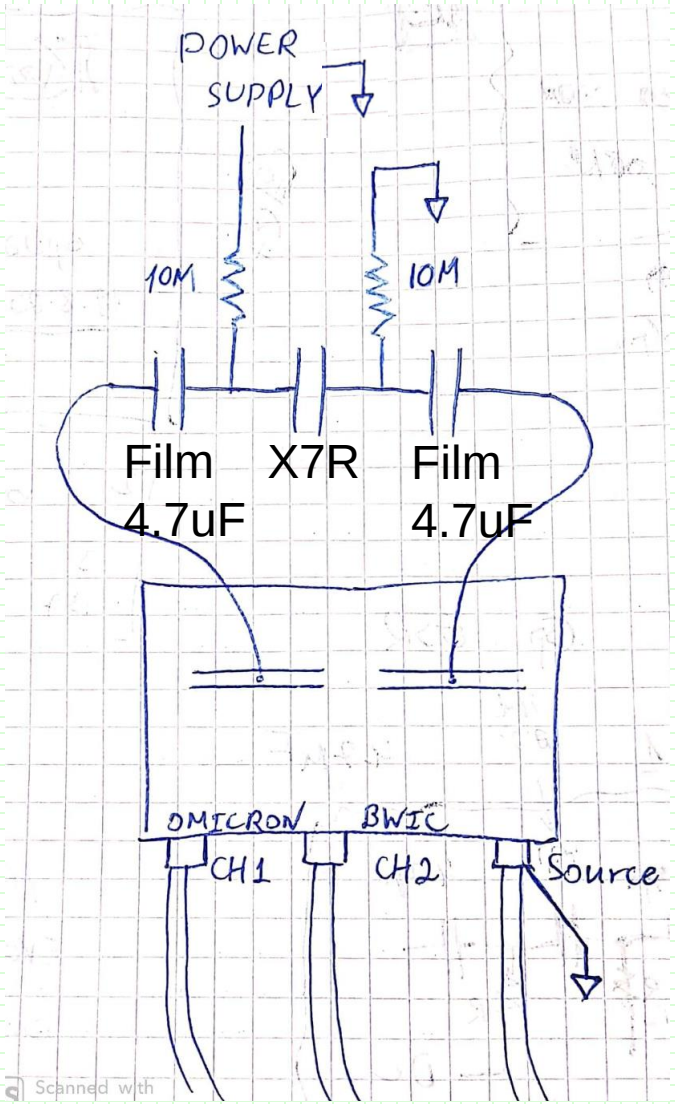


Results for Film Capacitor



Experiment Setup and results for X7R Capacitor





Submitted to PCIM - 2020

Losses in Ferroelectric Dielectric Ceramic Capacitors due to Electromechanical Resonances

Hermann Haag[1], André Mitterbacher[2], Florian Hämmerle[1]

[1] OMICRON electronics GmbH, Austria
[2] University of Applied Sciences Vorarlberg, Austria

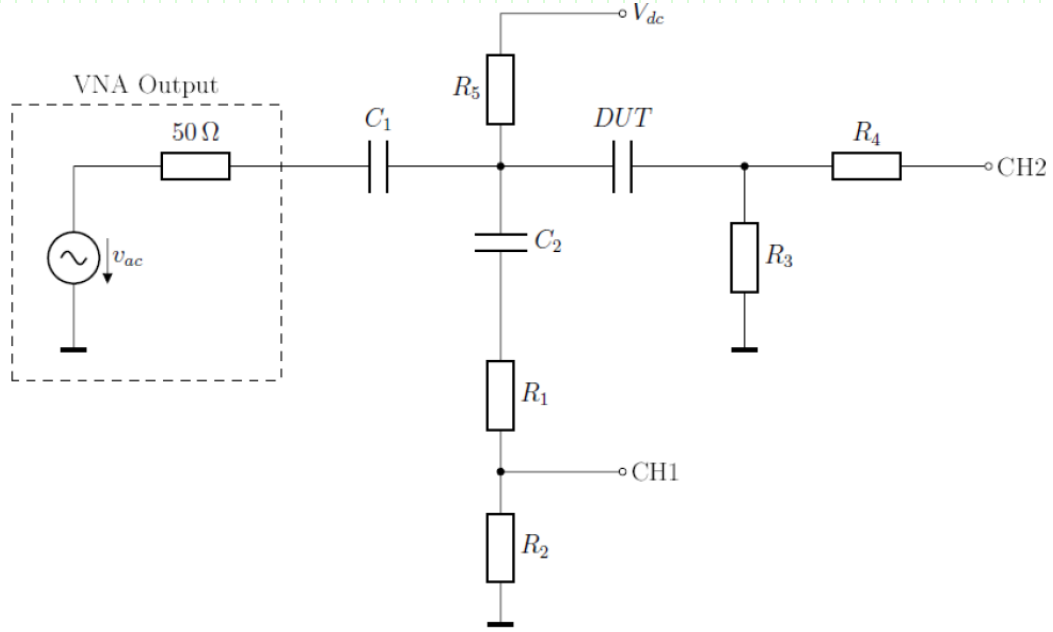


Fig. 1: Schematic of the DC biased ESR measurement

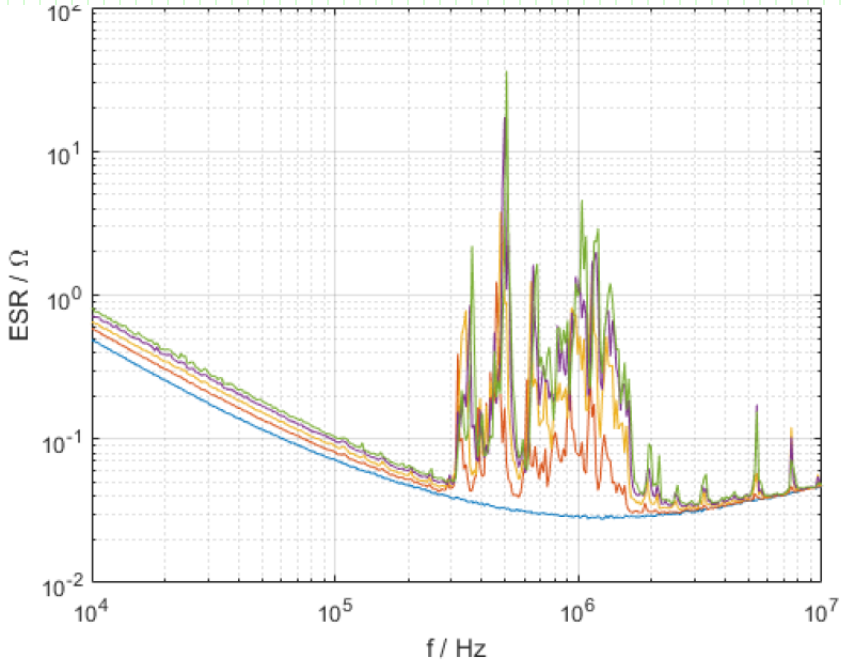


Fig. 2: ESR versus frequency of an X7R FDCC with different DC bias

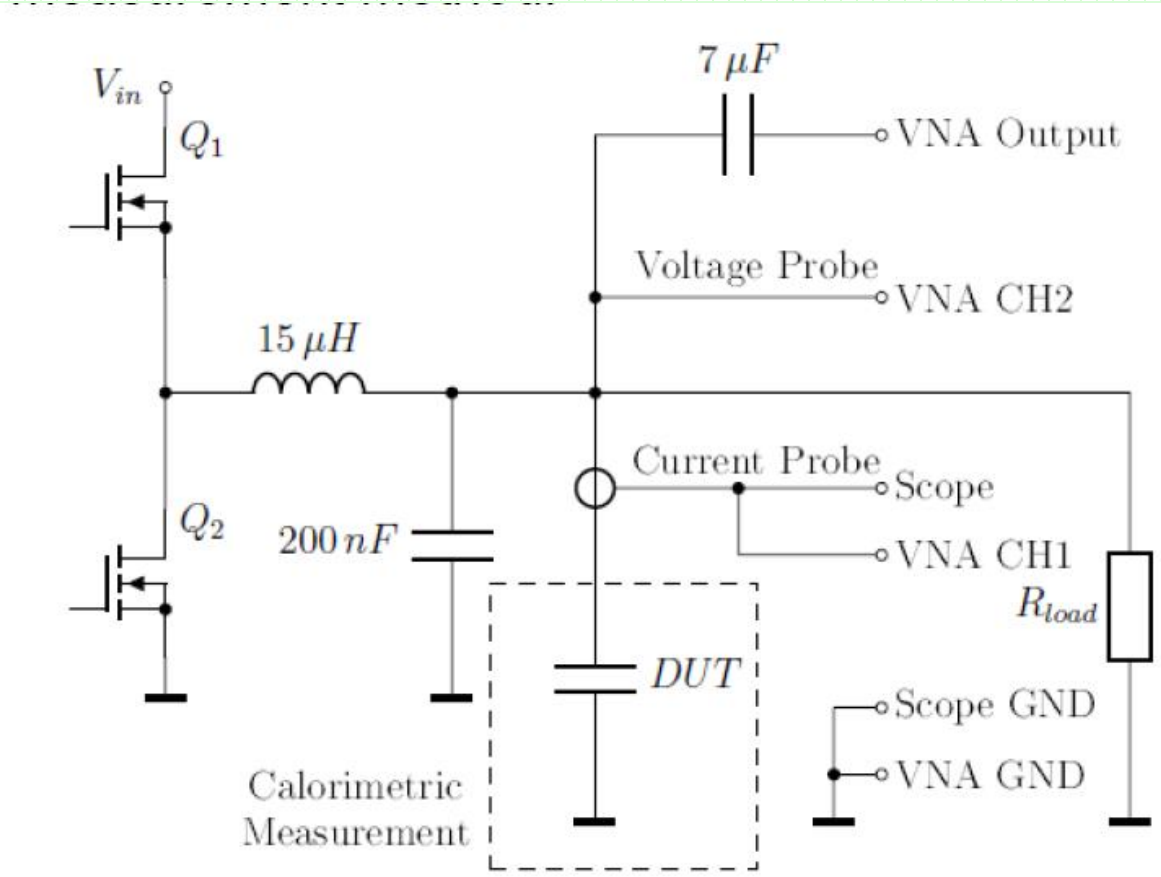


Fig. 3: Schematic of the loss measurement

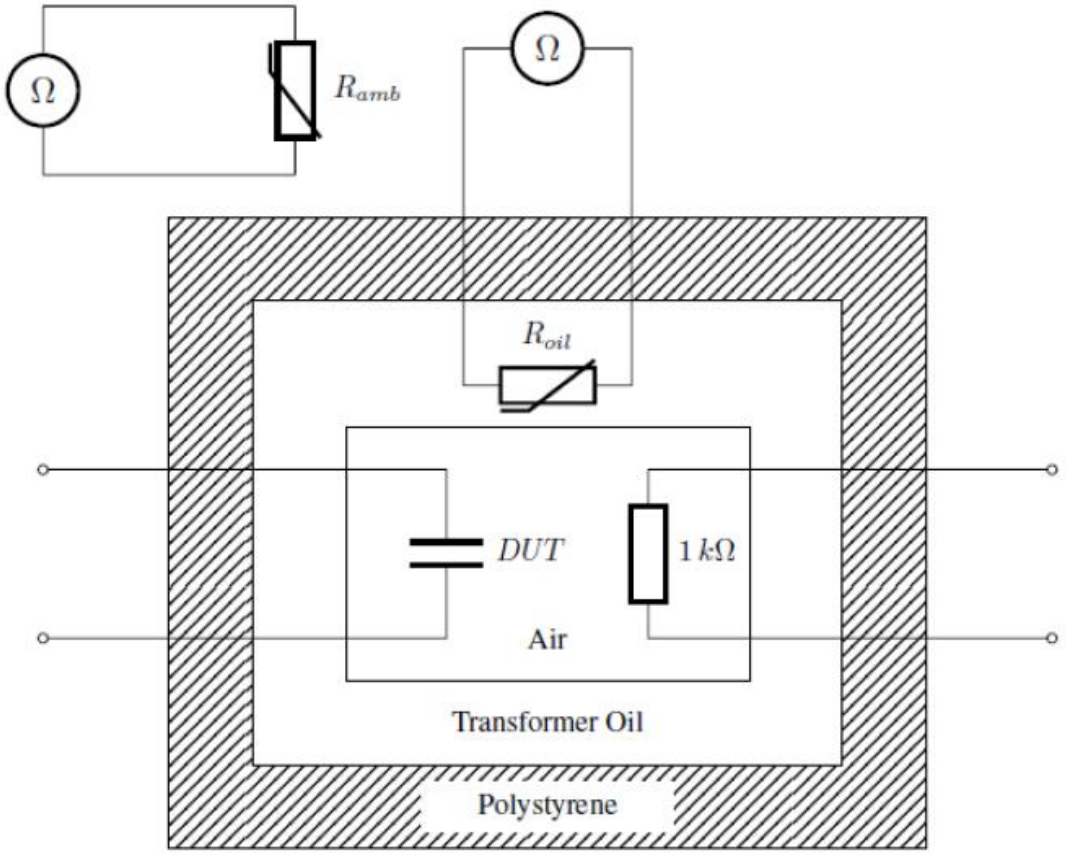


Fig. 4: Calorimetric loss measurement

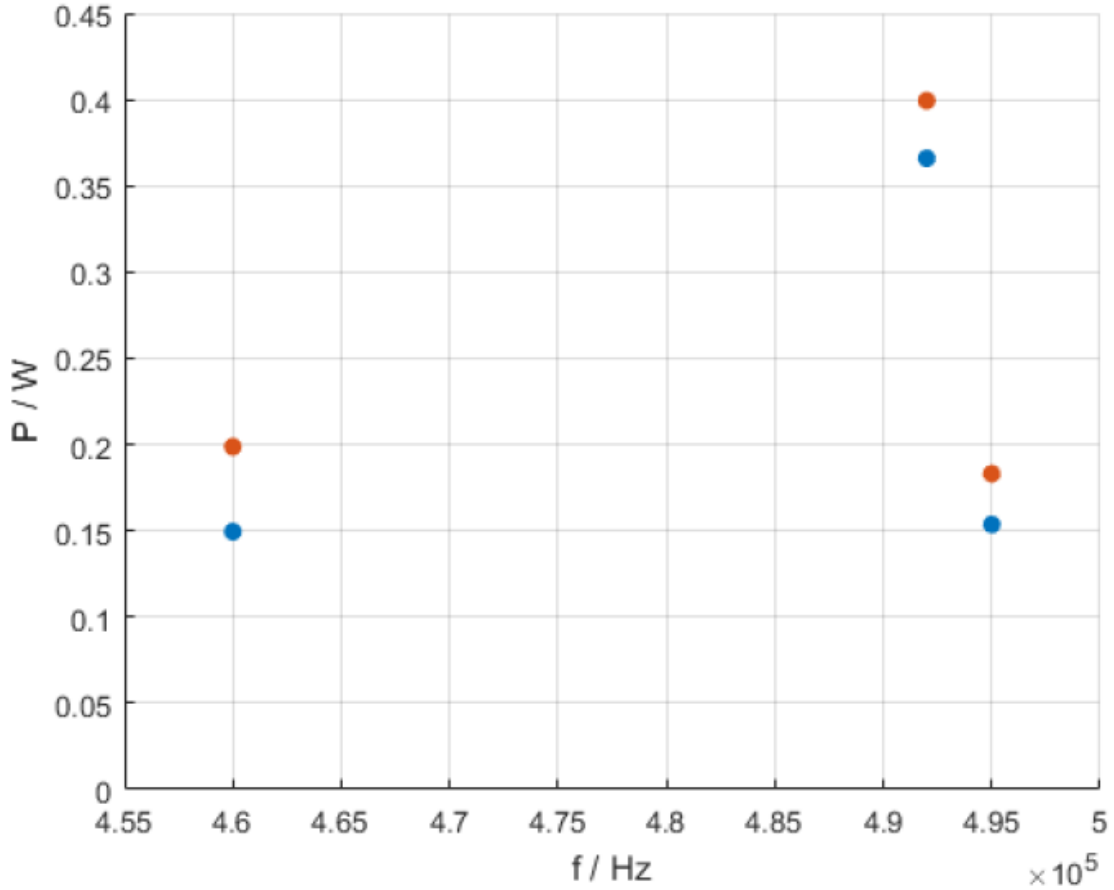


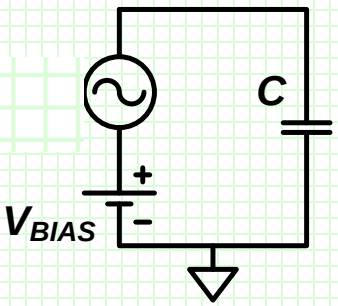
Fig. 5: Losses in the capacitor at three different frequencies. Blue: $P_{lossMeas}$. Red: $P_{lossCalc}$

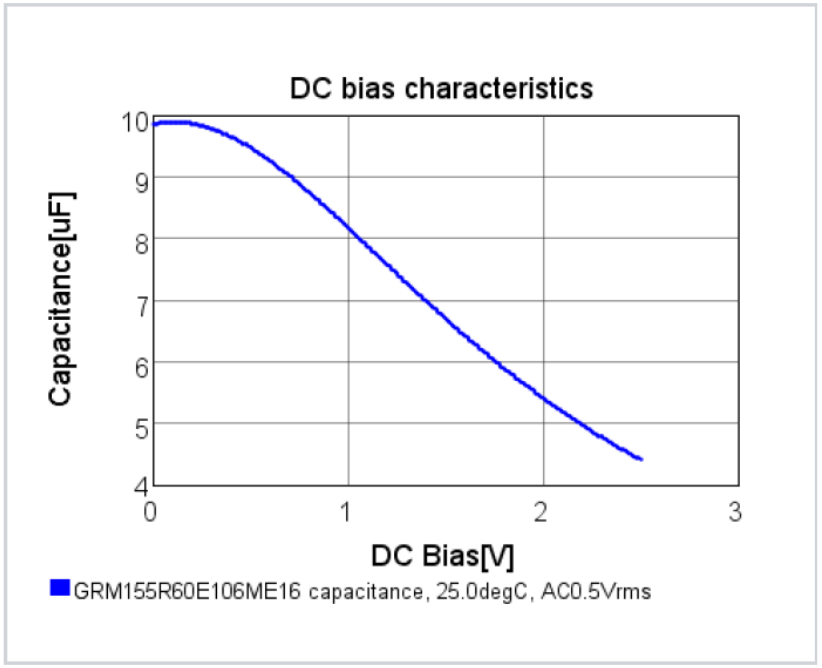
ESR and piezoelectricity of ceramic capacitors:
more research is required

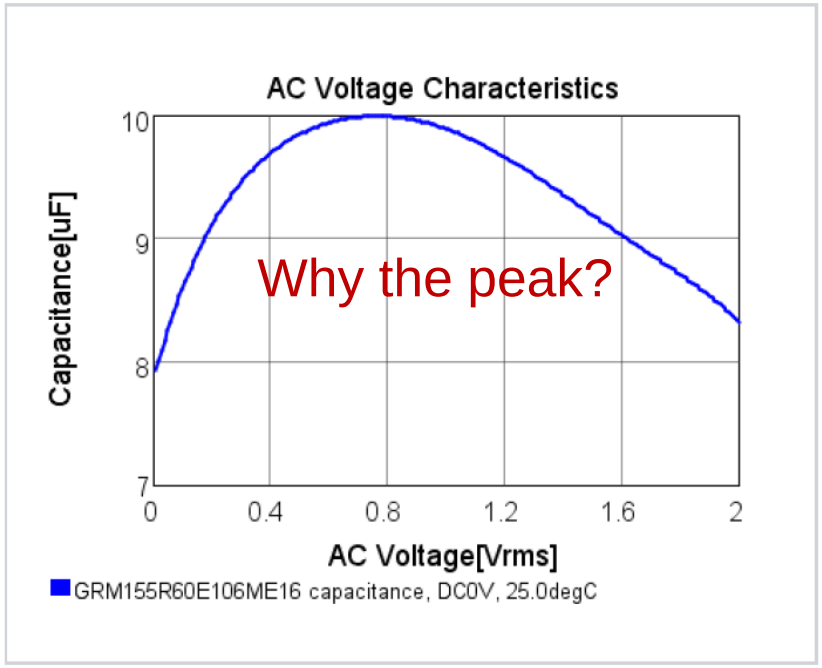
Nonlinear capacitors modeling

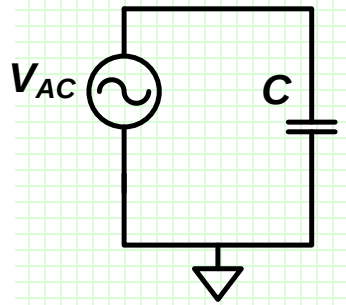
Capacitance definition

$0.5V_{rms}$









1kHz

Local, Small signal, C_d Large signal C_{ac}

Which model is correct?

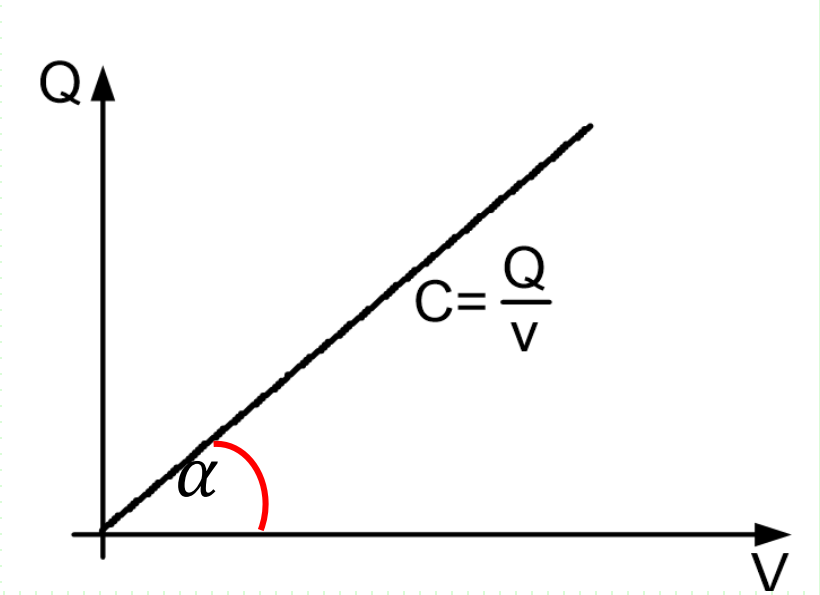
$$i = C(v)\frac{dv}{dt}$$

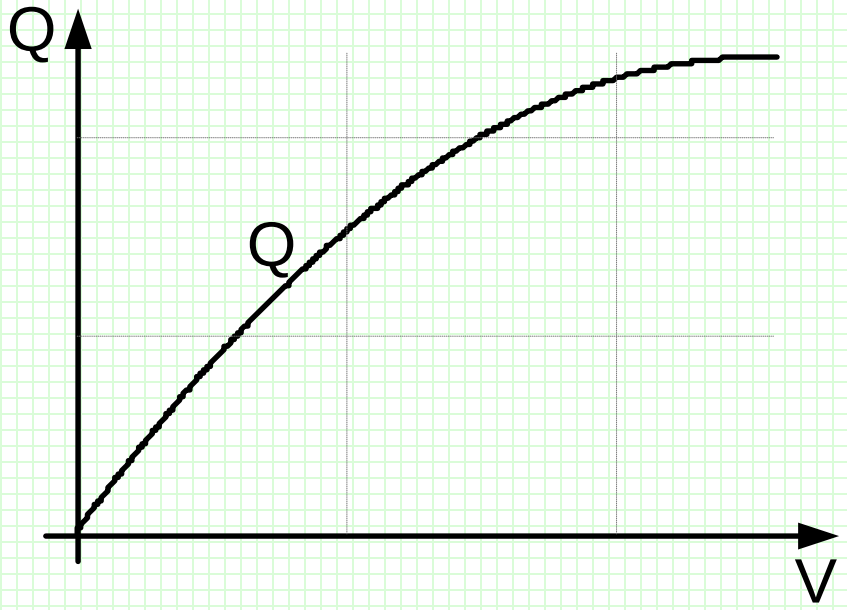
$$i = \frac{d\{C(v)\cdot v\}}{dt}$$

$$i = C(v)\frac{dv}{dt} + v\frac{d\big(C(v)\big)}{dt}$$

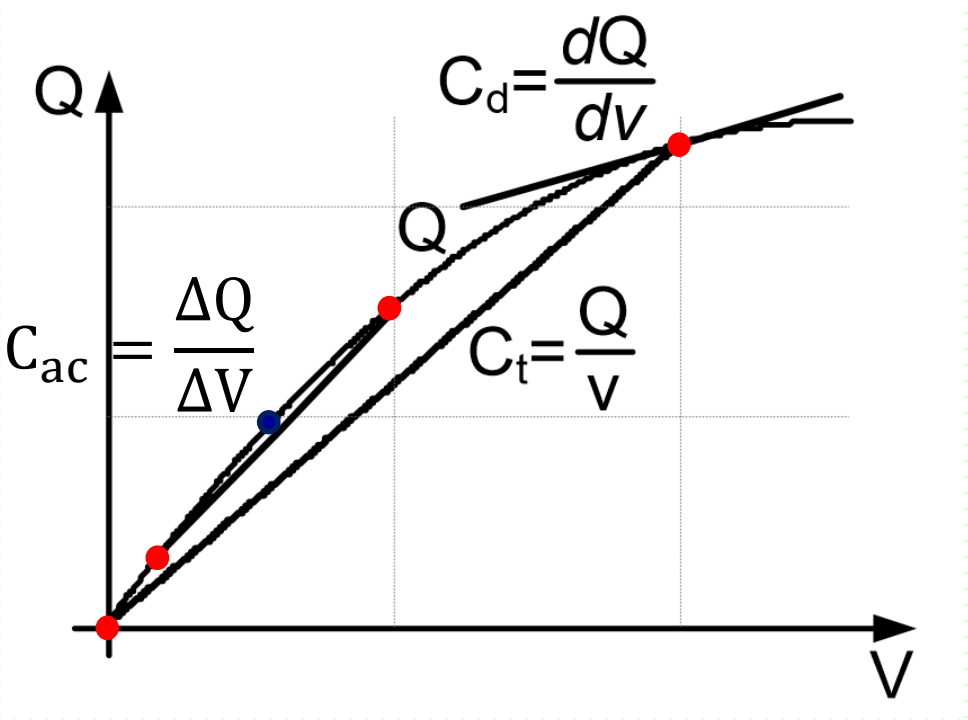
The fundamental property of a charge storing device - Q=f(V)

$$i = \frac{d\{Q\}}{dt}$$





Redefining ‘capacitance’

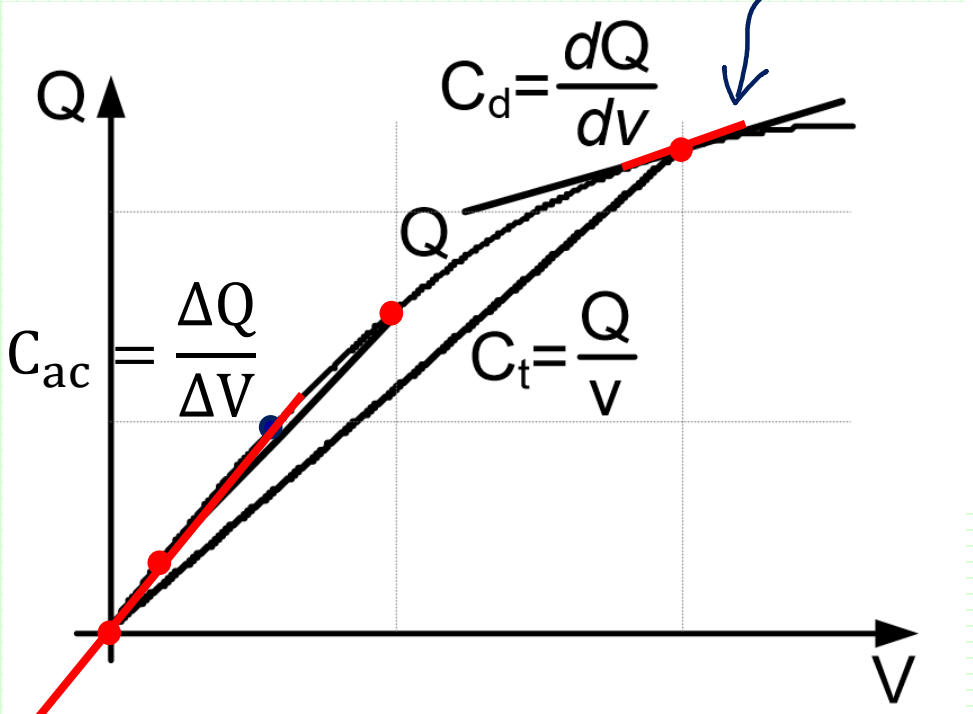


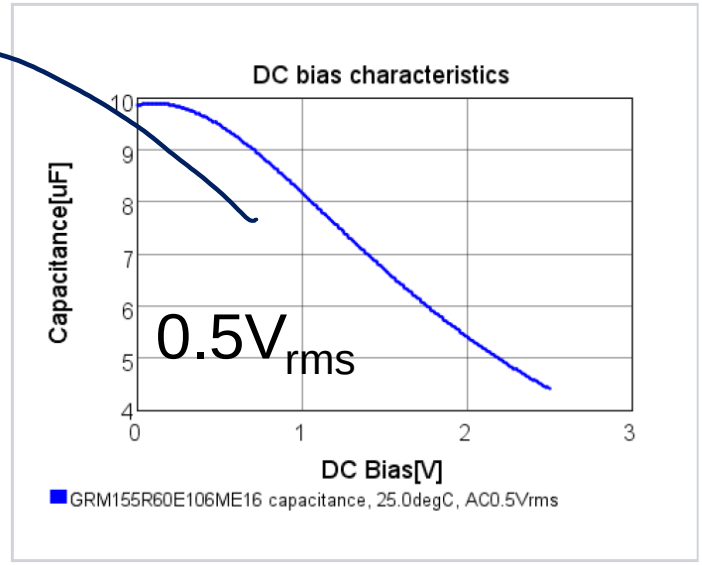
$$C_t(v) = \frac{Q(v)}{v}$$ Total Capacitance

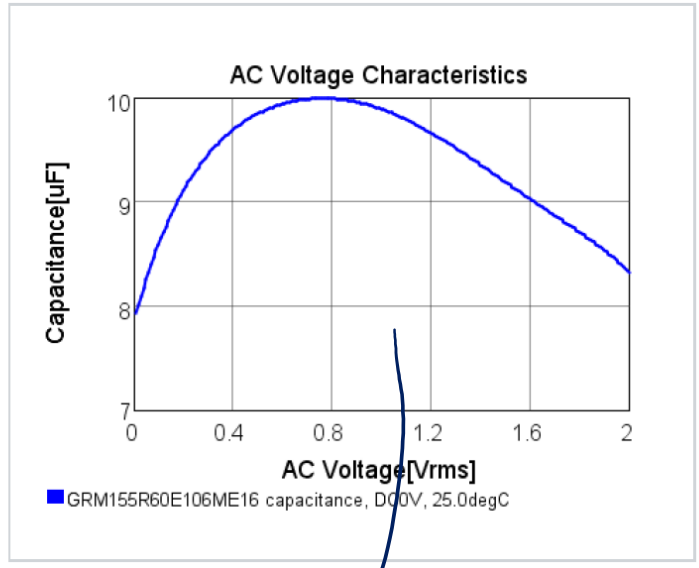
$$C_d(v) = \frac{dQ(v)}{dv}$$ Local Capacitance
Small signal

$$C_{ac}(v, A) = \frac{\Delta Q}{\Delta V}$$ Large signal Capacitance

Redefining ‘capacitance’







Cd

Cac

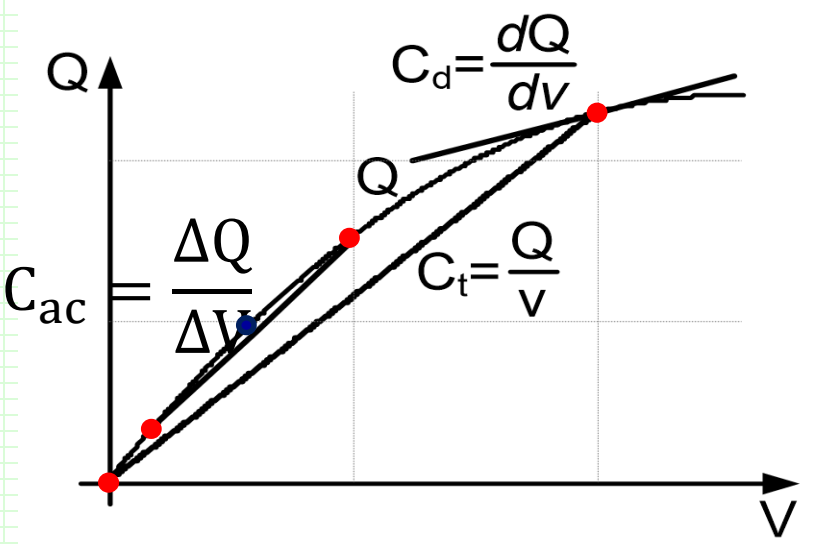
Total Capacitance

$$C_t(v) = \frac{Q(v)}{v}$$

$$Q(v) = vC_t(v)$$

$$i = \frac{d\{vC_t(v)\}}{dt}$$

$$i = C_t(v)\frac{dv}{dt} + v\frac{d\left(C_t(v)\right)}{dt}$$



$$C_t(v) = \frac{\int_0^v C_d(v)dv}{v}$$

Local Capacitance Small signal

$$C_d(v) = \frac{dQ(v)}{dv}$$

$$Q(v) = C_d(v)dv$$

$$\frac{dQ(v)}{dt} = C_d(v)\frac{dv}{dt}$$

$$i = C_d(v)\frac{dv}{dt}$$

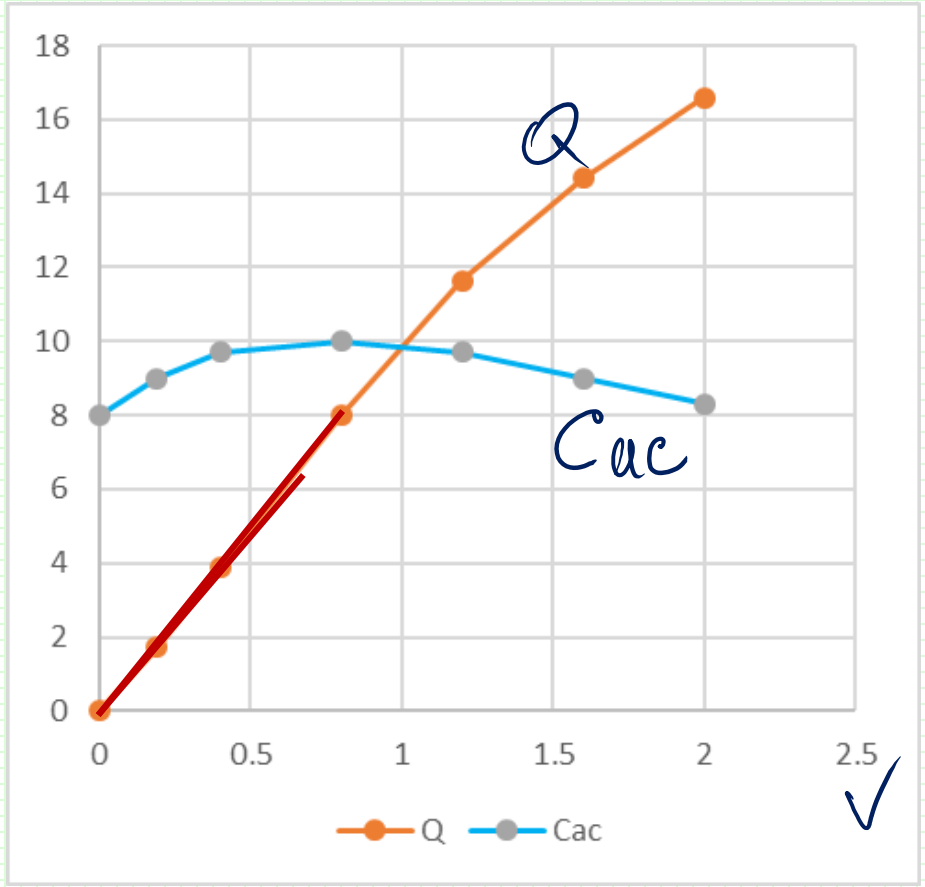
Conclusion: Both models are correct

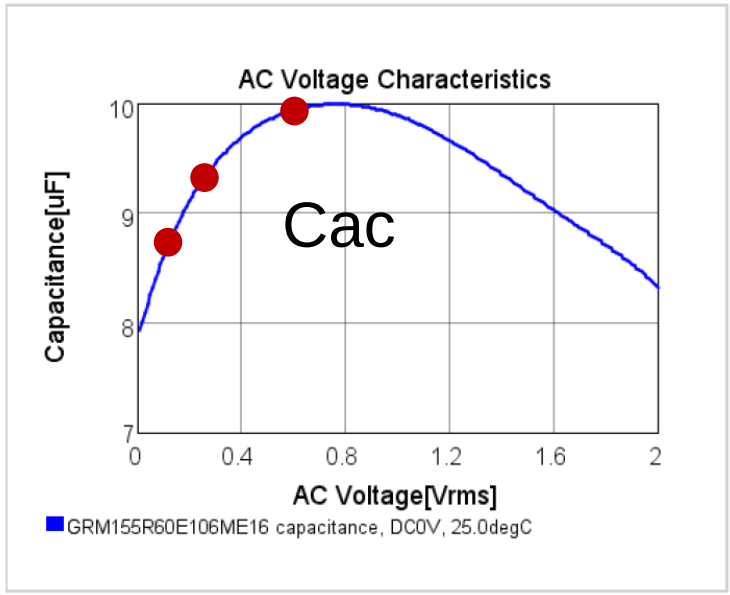
Provided that the ‘capacitances’ are defined properly

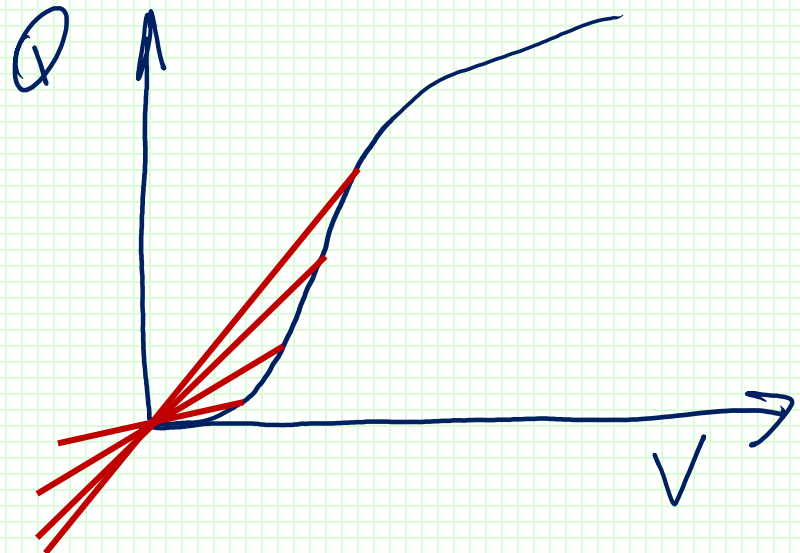
$$i = C_t(v)\frac{dv}{dt} + v\frac{d\left(C_t(v)\right)}{dt} \qquad i = C_d(v)\frac{dv}{dt}$$

$$C_t(v) = \frac{\int_0^v C_d(v)dv}{v}$$

So why the peak?







Thank you for your attention!