Parallel DCMs™

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Contents

Introduction

The DC-DC Converter Module (DCM) operates on a high frequency, double-clamped zero voltage switching (DC-ZVS) topology, which provides a revolutionary increase in density and efficiency compared to other complete DC-DC converter solutions. The DCM encapsulates isolation, regulation, thermal management, and fault monitoring in a single module. DCMs are available in two different packages: Converter housed in Package (ChiP) and Vicor Integrated Adapter (VIA) package. For more information on ChiP DCM capabilities and options, please see the application note "AN029: Single DCM as an Isolated, Regulated DC/DC Converter" and the Vicor web page for DCMs: www.vicorpower.com/dc-dc-converter-board-mount/dcm-dc-dc_converter.

When an application calls for more power than can be delivered by a single DCM, multiple DCMs can be put in parallel. This application note discusses the parallel operation of ChiP DCMs. Paralleling DCMs is straightforward, since the operation of each DCM in an array is nearly identical to that of a single DCM circuit (which is described in the DCM data sheets and the application note AN029: Single DCM as an Isolated, Regulated DC/DC Converter). In a parallel circuit, each DCM operates on its own load line, based on its share of the load; in general, the effect of adding DCMs in parallel is to remap that same load line over a higher current range, with no derating.

Current sharing between DCMs is automatically implemented. It is dependent on the individual DCM's output setpoints and load lines. Good load sharing among DCMs in an array is generally desired; however in most cases, it's not critical to accurately match the output setpoints, since DCMs are designed to operate without damage even in the case of a large sharing imbalance. An example of maximum sharing imbalance, between a DCM at full load and another DCM at minimum load is presented in this document (see section: "Special Application: Non-equal Trim Levels").

Despite not being required for operation, still it is better to optimize the current sharing, because that results in a more predictable aggregate load line and more equalized power dissipation. Equalizing power sharing across all DCMs also means that each DCM is operating at its lowest possible temperature, which results in better efficiency. To achieve good current sharing it is not necessary to have extremely accurate setpoints, since the load line has a bigger contribution to the output operating point vs. load than a small setpoint error; additionally, the DCM has a built-in negative temperature coefficient (see Output Voltage Regulation section below) which helps to further compensate for small current sharing imbalances.

Sample Circuit

An example of a circuit with four parallel DCMs is shown in Figure 1. In this circuit, the four DCMs have different input voltage sources (all referenced to the same –IN).

DCMs have on-board protection for input overvoltage and overcurrent, so the fuses F1-F4 shown in Figure 1 are only needed for applications that must pass safety approvals, such as CE Mark or UL60950. In that case, note that each DCM needs its own input fuse. For more information on fuse selection and recommendations, see the DCM data sheet.

Each DCM has to see at least $C_{OUT-MIN}$ local to its output pins, before any output inductors (and therefore closer to the DCM than to the junction of all DCM outputs). In arrays where all the DCMs are always started together, the array may have up to n* $C_{OUT-MAX}$ of total output capacitance (both local and bus capacitance). In arrays where DCMs can be started individually, the total capacitance seen by any DCM output (both local and bus capacitance) must be equal or below the $C_{OUT-MAX}$ of a single DCM. See sections "Startup" and "Support Circuitry and PCB layout" for more information.

For stability, to minimize ringing, and to provide optimal margin between the DCM's rated input low line and its input undervoltage fault protection threshold (UVLO), the source impedance of V_{IN} must be no more than half the combined effective input impedance of the DCM array. For example, for the DCM3623T50M17C2M00 at full output power (320W) and nominal efficiency (93%), the input power is 344W; at low line (16V) this corresponds to an equivalent input impedance of 0.744Ω (i.e. 162/344). For an array of four units, the combined input impedance is 0.186Ω, and the source impedance must be no higher than 0.093Ω. If this is not the case, the input filter circuit must compensate for the excessive impedance. A large electrolytic capacitor can be used at each DCM's input: specific information about filter design for each DCM model is provided in its corresponding data sheet (see "Line Impedance, Input Slew rate and Input Stability Requirements" in the datasheet). An additional useful resource for filter design is Vicor's online filter design tool, which can be found at the following link: http://app2.vicorpower.com/filterDesign/intiFilter.do.

For more information on component selection, see AN029: Single DCM as an Isolated, Regulated DC-DC Converter, and AN023: Filter Network Design for VI Chip® DC-DC Converter Modules.

Figure 1
Parallel DCM Circuit
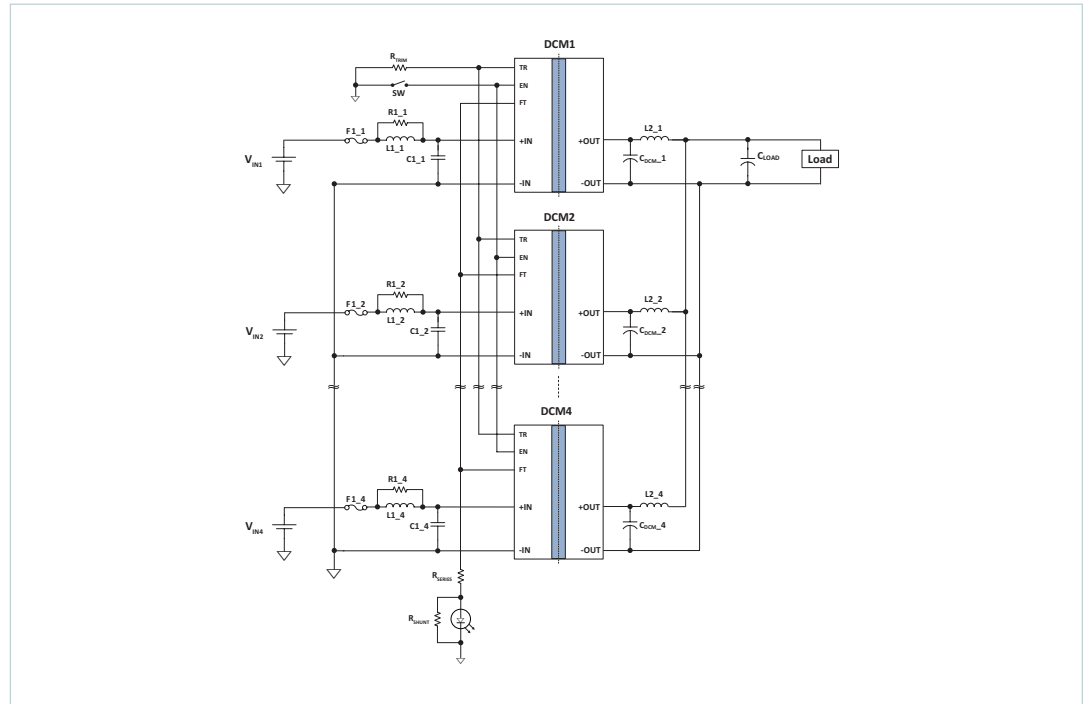
Output Voltage Regulation

As explained in the DCM™ data sheets, the DCM provides a regulated output voltage around a load line that is 5.263% of the nominal voltage referenced to full load. Decreasing the load causes the output voltage to rise.

Details regarding DCM Load Line Slopes and specified values

Specifying 5.263% at full load is the same as specifying the load line as having 5.0% of some no-load voltage. For example, with a 24V nominal output DCM,

$$V_{OUT\_NO\_LOAD} = V_{OUT\_FULL\_LOAD} \cdot (1 + 0.05263)$$

$$V_{OUT\_NO\_LOAD} = 24 \cdot (1 + 0.05263) = 25.26V$$

In the other direction:

$$V_{OUT\_FULL\_LOAD} = V_{OUT\_NO\_LOAD} \cdot (1 - 0.05)$$

$$V_{OUT\_FULL\_LOAD} = 25.26 \cdot (0.95) = 24V$$

Since the marketed $V_{OUT-NOM}$ refers to the full load voltage, to keep the literature consistent, the 5.263% figure will be used here.

An example of an ideal V_{OUT} vs. I_{OUT} plot for the DCM4623TD2H26F0T00 is shown in Figure 2, which is a modified version of one of the DCM™ data sheet figures (Figure 6 — Ideal V_{OUT} vs. load current, at 25°C case). This is an ideal plot because it does not consider the contribution of light load boosting, which is addressed separately.
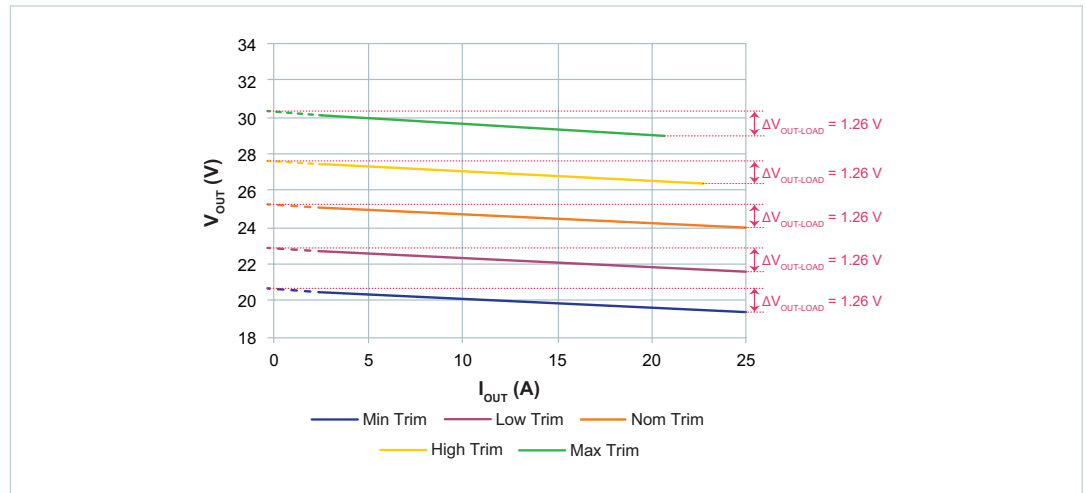
As shown in the figure, changing the trim value doesn't affect the slope of the load line; the slope is still 5.263% of the nominal output voltage at full load , which for the model used in this example corresponds to a $V_{OUT-LOAD}$ of 1.26V. The same is true of changes in temperature: voltage decreases with increasing temperature, but the slope of the output voltage transfer function doesn't change. (See "Overall Output Voltage Transfer Function" in the DCM data sheet.)

If the equivalent series resistance introduced by the DCM load line is needed, it can be calculated starting from the load line equation given in the DCM datasheet, in the section "Nominal Output Voltage Load Line." For example, the load line equation for the DCM4623TD2H26F0X00 (with nominal trim) is:

$$V_{OUT} @ 25° = V_{OUT\_FULL\_LOAD} + \Delta V_{OUT-LOAD} \bullet (1 - I_{OUT}/I_{OUT\_RATED})$$

Where:

- $V_{OUT\_FULL\_LOAD}$ is the voltage at full load and nominal trim,

- $V_{OUT-LOAD}$ is the rise of the "ideal" load line,

- I_{OUT} is the actual output current, and

- I_{OUT_RATED} is the rated output current in Amps (full load current).

The equation above can be rewritten as:

$$V_{OUT} @ 25° = V_{OUT\_FULL\_LOAD} + \Delta V_{OUT-LOAD} - \Delta V_{OUT-LOAD} \bullet (I_{OUT}/I_{OUT\_RATED})$$

Using typical values:

$$V_{OUT-LOAD} = 1.26V$$

$$V_{OUT\_FULL\_LOAD} = 24.0V$$

$$I_{OUT\_RATED} = 25.0A$$

and combining terms,

$$V_{OUT} @ 25° = 25.26 - (1.26/25.0) \bullet I_{OUT}$$

Where 25.26V is the "ideal" voltage at no load and nominal trim, which corresponds to the 24.0V

output at full load and nominal trim plus 1.26V for the load line.

$$V_{OUT} @ 25° = 25.26 - 0.0504 \bullet I_{OUT}$$

The equivalent series resistance in Ohms introduced by the load line, $V_{OUT-LOAD}/I_{OUT}$ (50.4mΩ in this example), can be referred to as $R_{INT\_LOADLINE}$.

Load Sharing

The primary objective of paralleling DCMs™ is to extend the loading capabilities beyond that of a single DCM. See Figure 3 for an example. The figure shows multiple DCMs operating along the same load line as a single DCM, but with the output current scaled proportionally with the number of DCMs in parallel. As implied in Figure 3, the failure of a single unit doesn't necessarily result in the array being brought down, if the array is sized as N+1 redundant relative to the maximum load. As in other cases, sharing is based mainly on the load line and to a lesser degree, the temperature coefficient, which is discussed next.

Parallel units with the same output setpoint (i.e., same trim value and same temperature), ideally would have their load lines perfectly overlap, and therefore their current sharing would be perfect. In reality, there might be a small difference in sharing due to the output voltage setpoint accuracy, which could cause the real load line of each DCM to move slightly from the ideal setpoint. This would cause some sharing imbalance: that is, a unit with a slightly higher output voltage setpoint would contribute a little more to the output current than a unit with a lower output voltage setpoint. Inaccuracy in the setpoint represents a small contribution to the load line, so the resulting sharing imbalance would be minor.

Figure 3
*Parallel DCMs Behave Like a Single DCM with a Higher Output Current*
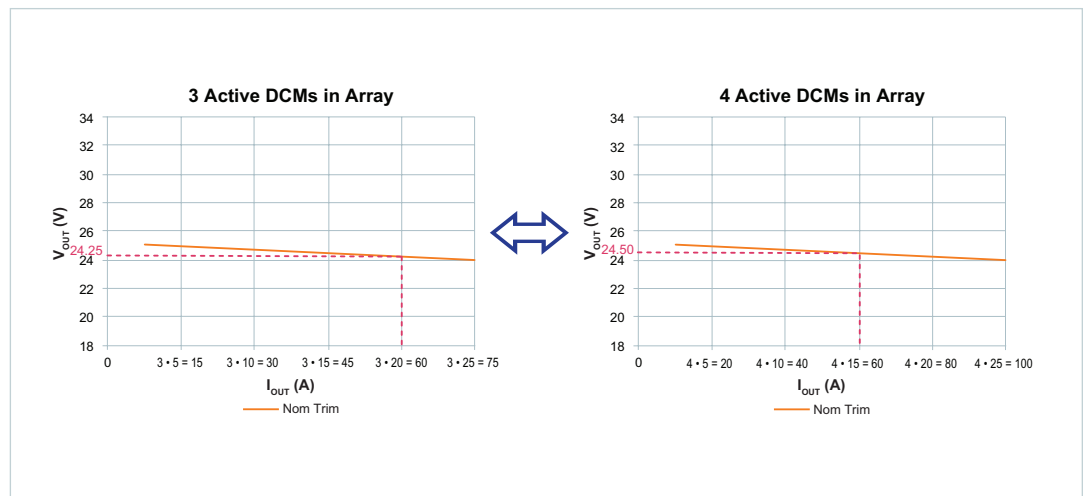
The maximum setpoint accuracy specified in the datasheet (%$V_{OUT\text{-}ACCURACY}$, ±2% for most models, -3% to +2% for some special DCMs) refers to the maximum variation of the setpoint over all possible operating conditions (line, load, trim and temperature). The setpoint accuracy for nominal conditions (nominal V_{IN}, nominal trim, full load, 25°C) is ±0.5% V_{OUT_NOM} (see the minimum and maximum values for "Output voltage setpoint" in the datasheet Electrical Specifications).

Temperature has a small, beneficial effect on current sharing. The DCM has a negative voltage-temperature coefficient (see "Overall Output Voltage Transfer Function" in the data sheet). If a unit is loaded more than others, its relative temperature tends to rise, which causes its output voltage to be reduced. Note that this change in setpoint does not affect the load line slope. Since the output voltages of the other parallel DCMs match that of the loaded DCM, their outputs would follow their load lines, increasing their share of the load current and bringing the circuit back to equilibrium.

DCMs operate well in parallel, even if their trim settings are not all the same. Unequal trim settings cause each DCM load line to start at a different y-intercept (see Figure 4); since their output voltages are forced to be the same value by the paralleled output connections, their currents will be different when the circuit achieves balance. The voltages and currents are maintained at those levels using the mechanisms described above. From Figure 4, it can be seen that setting the trim at different levels between units creates a mismatch in current sharing.
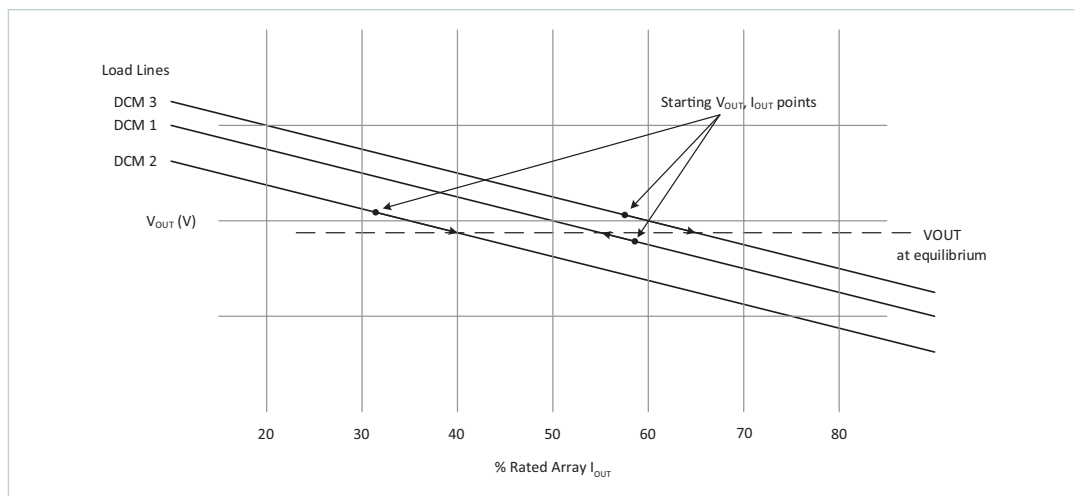
Sharing improves at the upper limit of the output power range. Because of the finite accuracy of the output setpoint, the output voltages won't be identical (see Figure 4) so as the output power increases, the DCM™ with the highest voltage will reach its maximum output current before the others. When that happens, it will operate as a constant current source. (The DCMs not in constant current will continue to regulate the output voltage).

For either trim/sharing scenario discussed above, the output ripple is typically reduced in a parallel DCM circuit compared to that of a single unit, because the DCMs aren't synchronized. That is, their switching periods are not in phase, so the combined outputs of parallel DCMs can behave like a single output with a higher effective switching frequency and lower ripple amplitude. In the best case, the switching periods of N parallel DCMs would be evenly staggered in time, so that the equivalent switching frequency would be $N*f_{SW\_STANDALONE}$. Since all DCMs would contribute equally to maintaining the output voltage, the output ripple would be $V_{OUT\_RIPPLE\_STANDALONE}/N$. In the worst case scenario, all DCMs would have the same frequency and be in phase, such that the equivalent switching frequency and total output ripple would be the same as that of a single DCM. In a real-world situation, the switching periods are randomly distributed, so the output ripple lies somewhere between the two extreme cases.

Startup

The startup behavior of a DCM array depends on the type of load: resistive or constant current.

For a resistive load, the load current increases as the DCM array output voltage rises. On startup, DCMs have a soft-start ramp when operated alone; in an array, the DCMs don't all turn on at the same time, so there will be an additional component of the soft-start ramp due to a subset of DCMs starting before the others. This is most notable when the DCMs are started from the application of V_{IN}, with a slow input dV/dt. During the soft start ramp, if the load current V_{OUT}/R_{LOAD} exceeds the combined current limits (I_{OUT-LM}) of the active DCMs, then those DCMs go into current limit and the startup ramp plateaus to $V_{OUT} = R_{LOAD} \bullet I_{OUT-LM}$ (assuming this V_{OUT} is above $V_{OUT-UVP}$, the minimum current-limited V_{OUT}, listed in the DCM datasheet). As additional DCMs turn on and "catch up" to the first group, they add current drive capability (that is, they increase the total current limit), and the output voltage increases to a higher level, given by the load resistance multiplied by the new total current limit. This continues until there are enough active DCMs to provide the full load current at V_{OUT_NOM}, allowing all DCMs to exit from current-limited operation.

With a constant current load, the load current remains the same even if the DCM output voltage decreases. At startup, a DCM has a load current capability of $I_{OUT-START}$, which is approximately 10% of the full load. If parallel DCMs were started from the application of VIN and the load current exceeded the sum of the current limits of the active DCMs (I_{OUT-LM}), the active DCMs would go into current limit, as in the case for the resistive load. In this case, the DCM output voltage would drop, because the load current would be greater than the current limit, so the output voltage would collapse. The higher the constant current setpoint of the load, the faster the DCM output voltage would collapse. In some extreme scenarios, V_{OUT} could collapse when the first DCM turned on, before additional DCMs could start driving the load.

To prevent this, the startup delay between units would have to be smaller than the current limit delay; that is, the time from the first to the last DCM™ turning on would have to be shorter than the time it would take the current limit of the first DCM to kick in. This can be done by using EN to start the DCMs. To summarize, for constant current loads, EN ensures that the turn-on delay between DCMs is smaller than the current limit delay of one DCM.

Special Application: Optimizing Current Sharing at High Temperature

Optimizing the current sharing between DCMs equalizes power dissipation. While DCMs still operate even when the load current is not balanced, equalizing power dissipation leads to higher efficiency, since generally speaking, efficiency is slightly reduced near the maximum operating temperature.

There is an uncommon condition where good load sharing across an array is required for operation. This happens when the circuit operates at a temperature and power that are high enough to force the use of the derating curve shown in Figure 25 of the data sheet. In these applications, good current sharing is important because a gross imbalance would increase the temperature of the overloaded part, which would decrease its maximum power. There are two scenarios:

- When operating at a temperature and power level that are far from the derating curve, a load imbalance causes a temperature difference, (which is partially compensated for by the temperature coefficient), but the maximum power does not change. In this case, a loading imbalance does not adversely affect the system.

- When operating close to or at the derating curve, a load imbalance causes the temperature of the overloaded part to increase, which decreases the maximum power the unit can tolerate without triggering over-temperature protection (OTP). If the power being processed by the unit is above the derated maximum power, the DCM in question will trigger OTP and shut down. The other units have to compensate for the power drop caused by the unit shutting down, so their temperatures increase, reducing their maximum output power that the remaining units can tolerate without triggering OTP. This can lead to a domino effect that can potentially cause each DCM to trigger OTP and shut down one by one until the whole the system shuts down. For these applications, good current sharing is required.

Special Application: Non-equal Trim Levels

Deliberately setting the programmed trim of DCMs in an array to different levels, (such that some units reach their current limit long before others), could effectively be used to extend the equivalent load line of the array over the entire array load rating. While this is not a common application, it shows how robust the DCMs are, even under non-ideal conditions.

As an example, consider two units in parallel, both with V_{OUT_NOM} = 20V (at full load) and 10A maximum current each. As previously explained, DCMs have a built-in load line that is 5.263% of the nominal output voltage from full load to no load. For the units in this example, the load line would be 20*(0.05263) = 1.0526V (see Figure 5). At nominal trim the DCM would show an output voltage of 20V at full load and 21.0526V at no load (excluding the possible contribution of light load boosting, which is discussed separately). For these two DCMs in parallel, with nominal trim, the contribution of the load line would go from 21.0526V at no load to 20V at full load (I_{MAX}). I_{MAX} would be 20A, the sum of the individual currents.

This example considers a simplified ideal scenario where the current limit inception point is at 100% rated I_{OUT}. In reality the current limit inception is variable based on line and temperature conditions; min, typ, and max values are provided in the DCM datasheet (Output current limit, page 5).

If one unit, DCM1, is taken out of the parallel circuit (array) and its trim increased to 21.0526V at full load, its load line would still be 1.0526V, but it would go from 21.0526V at full load to 22.1052V (21.0526V + 1.0526V) at no load (see Figure 5). Putting this DCM back into the original circuit, and increasing the load from the zero to the maximum, the nominally trimmed DCM (DCM2) would not contribute to driving the load until DCM1 reached an output voltage of 21.0526V. At that point, DCM1 would be at full load, while DCM2 would be at the highest setpoint of its load line (i.e. the point at the load line for which the unit outputs zero current). As the load is increased, DCM1 would go in to current limit and DCM2 would start driving the load, meaning that it would regulate the voltage based on its own load line. With the load at 20A, DCM2 would also be at full load and V_{OUT} = 20V. The voltage from no load to the full load for the array would have gone from 22.1052V to 20V; the equivalent load line of the array would be almost 10% (i.e., almost double the load line of a single unit).

This example is of little practical value, since it negates many of the advantages of putting DCMs™ in parallel, but it shows that DCMs would still function in a predictable manner even under these extreme conditions (as long as the cooling for the DCMs satisfies the limits in data sheet Figure 25, maximum dissipation versus case temperature).

Figure 5

Effect of Parallel DCMs with Different Trim Set Points on Load Line
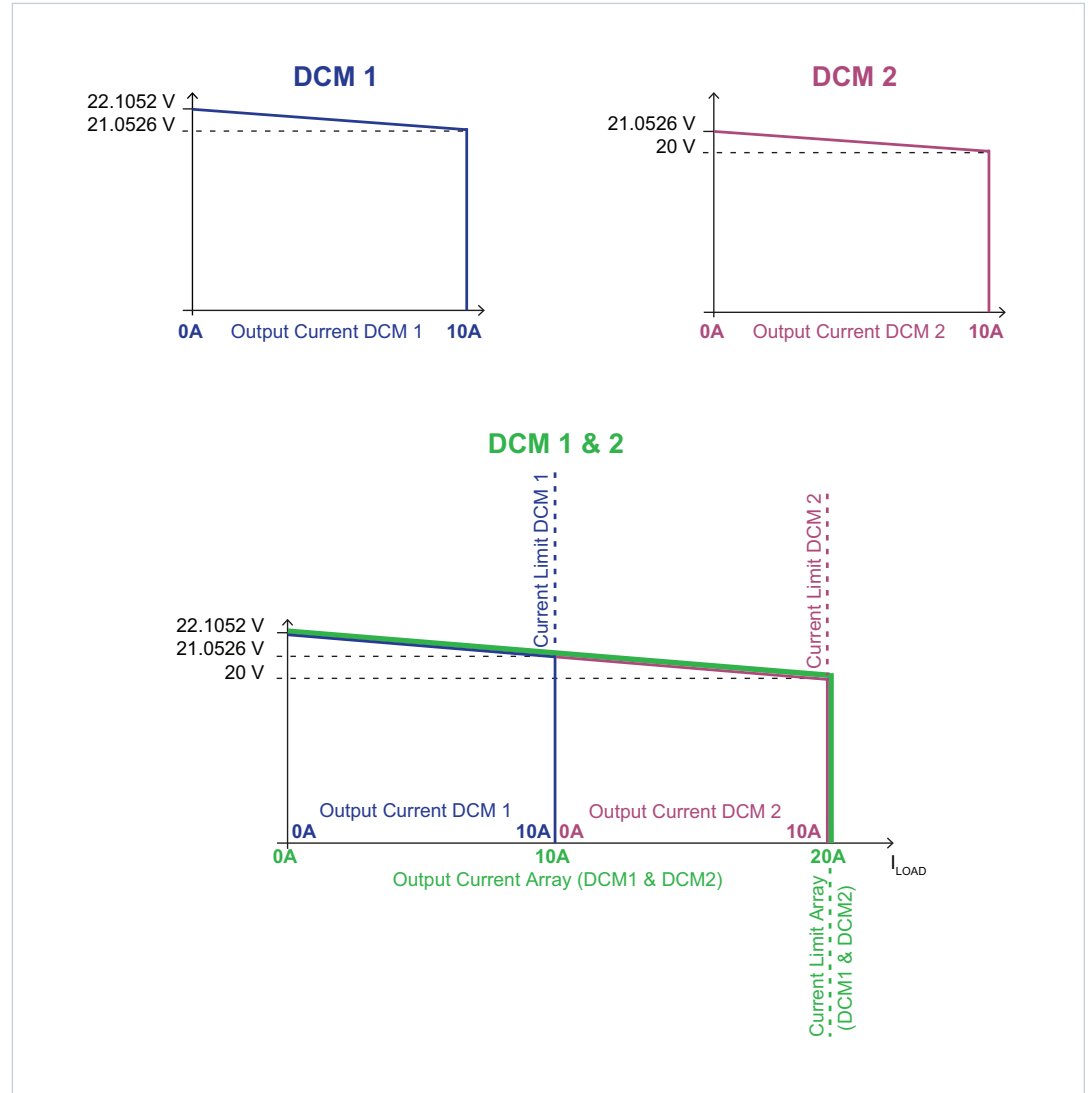
Support Circuitry and PCB Layout

Matching the trace impedances of the DCMs in an array isn't critical in most cases. From an output perspective, the DCM load line behaves as a series resistance which tends to trump any real series resistive effects of the PCB, assuming good design practices are followed.

Each DCM in an array should have an output inductor placed after its local output capacitor. The inductors help suppress beat frequencies that can be generated with DCM interconnected outputs. In some worst case scenarios, the circulating currents among DCM outputs with no decoupling inductors can inadvertently trigger a fault protection mechanism. The inductors also decouple each DCM and its local output capacitor from any bulk load capacitor as well as the local capacitors of other DCMs in the array. Without the inductors, the total load capacitance would be limited to that which is within the $C_{OUT-EXT}$ range of a single DCM.

A properly sized output inductor guarantees sufficient decoupling for the DCM to turn on within rated output capacitance even for the worst case scenario of maximum turn on delay between the DCMs in an array. Recommended output inductor values for each DCM model are provided in the DCM data sheet under "Array Operation".

In addition, as explained in the DCM™ datasheets, an input decoupling network is needed to facilitate paralleling. Each DCM needs a separate input filter; additionally, for applications that require common mode noise rejection on the input, a common mode choke should be added to the input side of each DCM. See "Array Operation" in the datasheet for recommended design specific component values for each DCM.

The TR and the EN pins should be equipped with low pass filters to avoid high frequency interference on the control signals. Noise on TR might cause unwanted oscillations on the output voltage. Noise on EN might cause the DCM to turn off and on at unwanted times. When designing a circuit to drive TR, it's better not to load the pins with a capacitor, but to add a resistor (R2 in Figure 6) so that TR isn't coupled to the capacitor directly, which could create a resonant tank between the capacitor, the lead inductance, and the internal bypass capacitor (which isn't shown in Figure 6). The same filter design can be used also for EN (however R2 in this case is not required since there is no internal resonant tank on EN).

EN is a simple on/off input; each DCM has a pull-up resistor $R_{ENABLE-INT}$, which is approximately 10kΩ (for an array with N DCMs in parallel, the internal pull-up resistors will be in parallel as well, lowering the equivalent pull-up resistance of TR an EN for the array to 10kΩ/N). The values of R1 and R2 need to be such that the voltage on EN is less than the specified minimum of $V_{ENABLE-DIS}$ = 0.99V, keeping in mind that if one filter circuit is used for all of the EN pins, the pull-up resistors of the DCMs would be in parallel, so R1 and R2 would have to be chosen accordingly.

Calculating the resistor values for TR is a bit more complicated, since the pin voltage is much more critical. The easiest solution is to measure the trim pin voltage VTR directly and set the value of Vs so that VTR is correct. If one filter is used for all DCMs in parallel, the values of R1 and R2 need to be chosen for the parallel combination of pull-up resistors.

Figure 6
Filter Circuit for EN or TR Pin
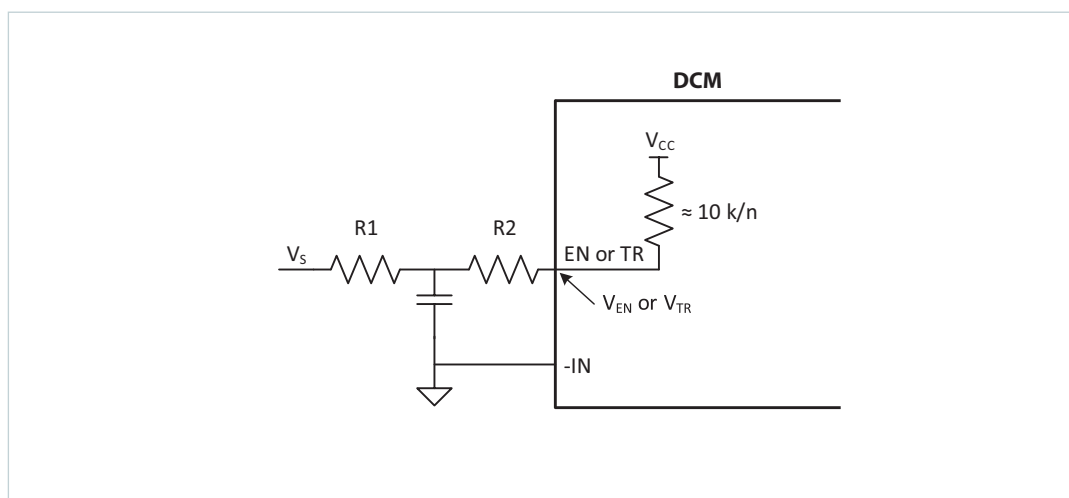
The DCM powertrain switching noise frequency is significantly higher than the trim update frequency, so the filter does not need to be finely tuned or very accurate. The trim bandwidth is around 30Hz, while primary source of noise is the switching of the main powertrain, often close to 1MHz depending on the DCM model. A low pass filter with a cutoff frequency of less than 1kHz would introduce sufficient attenuation to help avoid any risk of interference from switching noise, with just a simple 1st order filter network.

FT pins can be directly bussed (as previously shown in Figure 1) because of the open-drain structure. When the array is operating normally and no fault is present, FT is pulled up to 3.3V and the aggregate pull-up resistance of FT is 499kΩ/N, so an external pull-down (R_{SHUNT} of Figure 1) needs to overcome that combined pull-up.

The pull-down value should be sized to allow the external fault detection sub-circuit to robustly resolve the normal operating mode status versus a faulted state. A fault condition could affect all, or just one DCM, so the total drive high current must still be limited to the 4mA of a single DCM (the current limit is determined by the value of value of R_{SERIES} previously shown in Figure 1).

Conclusion

Parallel DCMs™ have many benefits: increased current, redundancy, and increased reliability - all with no derating. The theory of operation is primarily an extension of the operation of a single unit, with some additional considerations to be sure that current sharing is optimized, so that the circuit achieves maximum efficiency.

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